Björn Almeroth

Aspects of Analog-to-Digital Conversion in Modern Receiver Architectures

Beiträge aus der Informationstechnik

Mobile Nachrichtenübertragung
Nr. 72

Björn Almeroth

Aspects of Analog-to-Digital Conversion in Modern Receiver Architectures

VOGT

Dresden 2015

Bibliografische Information der Deutschen Nationalbibliothek
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über http://dnb.dnb.de abrufbar.

Bibliographic Information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at http://dnb.dnb.de.

Zugl.: Dresden, Techn. Univ., Diss., 2015

Die vorliegende Arbeit stimmt mit dem Original der Dissertation „Aspects of Analog-to-Digital Conversion in Modern Receiver Architectures“ von Björn Almeroth überein.

Gesetzt vom Autor

ISBN 978-3-938860-89-2

Jörg Vogt Verlag
Niederwaldstr. 36
01277 Dresden
Germany

Phone: +49-(0)351-31403921
Telefax: +49-(0)351-31403918
e-mail: info@vogtverlag.de
Internet : www.vogtverlag.de

Technische Universität Dresden

Aspects of Analog-to-Digital Conversion in Modern Receiver Architectures

Björn Almeroth

von der Fakultät Elektrotechnik und Informationstechnik der
Technischen Universität Dresden

zur Erlangung des akademischen Grades eines

Doktoringenieurs

(Dr.-Ing.)

genehmigte Dissertation

Vorsitzender:	Prof. Dr.-Ing. habil. Renate Merker
Gutachter:	Prof. Dr.-Ing. Dr. h.c. Gerhard P. Fettweis
	Univ.-Prof. Dr. rer. nat. Friedrich K. Jondral
Tag der Einreichung:	02. Februar 2015
Tag der Verteidigung:	07. Mai 2015

Abstract

The design paradigm for wireless radio terminals has experienced major changes in the last decades. Novel transceiver design principles encourage to move the digital signal processing closer to the antenna while reducing the amount of analog off-chip components. This design methodology gives the ability to built fully reconfigurable radios which are capable of operating at any frequency band and with any communication standard. As a consequence thereof, the requirements on the remaining analog components increases while the overall power consumption of the radio has to remain at the same level. A key component in every modern receiver architecture is the analog-to-digital converter (ADC). It faces even tougher specifications in the sampling rate and the quantization resolution compared to conventional receivers due to the reduced analog processing.

In this work, we investigate the process of analog-to-digital conversion in the light of direct bandpass (BP) signal sampling in detail. The behavior at each stage of the ADC is studied, basic performance limitations are discussed and a framework to determine feasible parameters is proposed. This work simplifies the parameterization of the bandpass sampling ADC (BP-ADC) and can be used to explore novel aspects in receiver design. For this purpose, the ADC is split into its two basic blocks: sampling and quantization. For BP sampling, the sampling stage is of fundamental importance as it deals with the time-discretization and the down-conversion of the desired signal simultaneously. In particular, we focus on the impact of realistic sampling circuits, i.e., sample-and-hold or track-and-hold, on the signal-to-noise ratio (SNR) of the desired receive signal. Furthermore, the problem of sampling jitter is investigated and its limitations on the SNR of the BP-ADC are shown. Finally, a framework to find feasible ADC configurations is proposed. It was found that considering the filter characteristics of the sampling circuit is indispensable for BP-ADCs. This property was often neglected for such applications. Moreover, the BP-ADC needs to comply with the certain sampling jitter requirements and a minimum quantization resolution to ensure a predefined

noise figure of the receiver. The obtained sets of feasible ADC parameters give a prediction on the expected power consumption and allows the selection of an appropriate ADC topology.

This work is enhanced by an advanced receiver architecture, which inherently compensates random phase rotations due to imperfect down-conversion mixing with jittered sampling. It is shown that using a shared clock signal with the same phase noise realization for the mixer and sampler dramatically improves the SNR performance of the receiver without any additional digital post-processing.

Kurzfassung

Die klassischen Paradigmen für den Entwurf mobiler Sender- und Empfängerarchitekturen im Mobilfunk haben in den letzten Jahrzehnten tiefgreifende Veränderungen erfahren. Neuartige Entwurfskonzepte für moderne Empfängerarchitekturen sehen eine frühzeitige digitale Signalverarbeitung, nahe der Empfangsantenne, vor. Die entwickelten Konzepte haben das Ziel die Anzahl an analogen, nicht integrierten Komponenten zu reduzieren. Gleichzeitig ermöglichen Sie die Umsetzung eines voll konfigurierbaren Radios, welches eine Vielzahl an Frequenzbändern und verschiedene Kommunikationsstandards verarbeiten kann. Als Konsequenz der frühzeitigen Digitalisierung des Empfangssignals müssen die Komponenten des Empfängers deutlich höheren Anforderungen, bei nahezu gleichen Leistungsverbrauch, genügen. Eine Schlüsselkomponente jeder modernen Empfängerarchitektur ist der Analog-zu-Digital Wandler (ADC). Dessen Spezifikationen bezüglich der Abtastrate, Genauigkeit des Abtastzeitpunktes und der Quantisierungsauflösung sind deutlich höher anzusetzen, vergleicht man diesen mit konventionellen Empfängerstrukturen. Dies resultiert vor allem aus der Verschiebung einzelner analogen Verarbeitungsschritte in die digitale Domäne.

Im Rahmen dieser Arbeit wird das Konzept der Analog-zu-Digital Wandlung, mit den Fokus auf die Direktabtastung von Bandpass (BP) Signalen, untersucht. Hierfür wird das Verhalten des ADCs stufenweise betrachtet, die grundlegenden Faktoren der Leistungsbegrenzung diskutiert und ein Rahmenwerk zur Parametrisierung des ADCs vorgestellt. Mit Hilfe dieser Arbeit wird die Auswahl geeigneter Parameter des ADCs zur Direktabtastung von BP Signalen vereinfacht. Dies kann wiederum dazu genutzt werden, neuartige Konzepte für moderne Sender-Empfängerarchitekturen zu entwickeln. Dabei wird der ADC zunächst in seine zwei Grundbestandteile eingeteilt: Abtastung und Quantisierung. Die Abtastung ist von grundlegenden Interesse für den Empfang von BP Signalen, da sie sowohl die Zeitdiskretisierung als auch das Heruntermischen des gewünschten Signals beschreibt. Die vorliegende Arbeit fokussiert sich hierbei vor allem auf den Einfluss von realistischen Abtastschaltungen (Sample-and-hold, Track-and-hold). Des Weiteren wird das Signal-zu-Rauschleistungsverhältnis (SNR) vor und nach der Analog-zu-Digital Wandlung untersucht. Neben den deterministischen Eigenschaften der Abtastung wird auch der Einfluss von Abweichungen vom idealen Abtastzeitpunkt (Abtastjitter) für BP Signale

analysiert. Daraus folgend werden wesentliche Limitierungen des Bandpass ADC (BP-ADC) abgeleitet. Abschließend wird ein Rahmenwerk zur Berechnung möglicher Parameter des BP-ADC vorgeschlagen. Dabei wurde festgestellt, dass das Einbeziehen der Filtercharakteristik des Abtast-Halte-Gliedes für den Empfang von BP Signal mit Techniken der Unterabtastung notwendig ist. Diese Eigenschaft wird oftmals vernachlässigt und führt zu einer deutlich Reduzierung der Leistungsfähigkeit des BP-ADCs. Neben der Filtercharakteristik muss für eine vorher festgelegte Rauschzahl des Empfängers sichergestellt werden, dass sowohl die Anforderungen an Abtastjitter als auch eine minimale Quantisierungsauflösung eingehalten werden. Die daraus resultierenden Parameter des BP-ADCs können dazu genutzt werden die Leistungsaufnahme neuartiger Empfängerkonzepte abzuschätzen und geeignete ADC Topologien auszuwählen.

Zusätzlich zu der Untersuchung des BP-ADCs wird in der vorliegenden Arbeit eine neuartige Empfängerarchitektur vorgestellt, welche den Effekt einer zufälligen Phasenrotation durch nicht-ideales, fehlerhaftes Heruntermischen mittels Abtastjitter inhärent kompensiert. Es wird gezeigt, dass das SNR durch die Nutzung eines gemeinsamen Taktsignals mit gleicher Realisierung des Phasenrauschens für Mischer und Abtaster deutlich gesteigert werden kann. Hierzu wird keine weitere digitale Nachverarbeitung des Empfangssignals benötigt.

Acknowledgement

The contributions of this work are based on the research work carried out during my time as a research associate at the Vodafone Chair Mobile Communications Systems at the Technische Universität Dresden. First of all, I wish to express my gratitude to Professor Gerhard Fettweis for giving me the opportunity and to continuously support my work. Without your motivation, your encouragement and your expertise, it wouldn't be possible to write this thesis. I also want to thank my second reviewer Professor Friedrich K. Jondral for the interest in my research topic and for the valuable comments.

I highly appreciate the continuous support of the CRC HAEC and my industry project partner Ericsson Nuremberg (former ST-Ericsson). All persons involved always gave very valuable theoretical and practical inputs which help me to understand several research topics in more detail. I will always retain these memories of the cooperation with all project partners.

I also want to thank all colleagues and friends from the chair. You have always supported and motivated me in my research. Moreover, I would like to highlight the nice time we spent together during our cultural dinners. I am indebted grateful to Stefan Krone, Meik Dörpinghaus and Alexandros Pollakis for proof-reading my thesis. In addition, I would like to thank all members of my research group: Lukas, Najeeb, Walter, Jan, Rohit, and Nicola.

Last but not least, I thank my close friends from Dresden and Eisenberg for the time we spent in the last years. Without this work-life balance, it wouldn't be such a memorable time of my life. The accomplishment of this dissertation wouldn't be possible without the love and support of you - my true friend Anne. I also truely appreciate the patience and the trust of my parents and family.

Folks, I enjoyed every single day with all of you!

Dresden, May-07, 2015 Björn Almeroth

Contents

Abstract / Kurzfassung iii

Acknowledgement vii

Contents ix

1 Introduction 1
- 1.1 Motivation and Background 1
- 1.2 Scope of the Thesis 3
- 1.3 Outline and Main Contributions 4

2 An Overview of Modern Receiver Architectures 7
- 2.1 Homodyne and Superheterodyne Receiver Architectures . . . 10
- 2.2 Direct-RF-Sampling Receiver Architectures 14
- 2.3 Analog-to-Digital Converters 19
- 2.4 Prospects and Challenges of Direct-RF-Sampling Receivers . . 24
- 2.5 Summary 27

3 Direct-RF-Sampling with Realistic Sampling Circuit Models 29
- 3.1 Model of the Voltage and Charge Sampling Circuit 30
- 3.2 System Model 38
- 3.3 Performance Evaluation 41
- 3.4 Application Example 43
- 3.5 Summary and Conclusions 46

4 Direct-RF-Sampling with Sampling Time Errors 47
- 4.1 Model of Sampling Jitter 49
- 4.2 Dominant Jitter Type for Voltage and Charge Sampling Circuits 53
- 4.3 Signal-to-Noise Ratio and Jitter Requirements 58
- 4.4 Application Example 61
- 4.5 Summary and Conclusions 63

5 An Advanced IF Receiver Architecture employing Shared Clock Signals **65**
5.1 System Model 68
5.2 Impact of a Shared Clock Signal on the Receiver Performance 73
5.3 Performance Evaluation 78
5.4 Summary and Conclusions 80

6 Framework for the Parameterization of the Analog-to-Digital Converter **83**
6.1 Structure of the Framework and its Opportunities 85
6.2 Performance Evaluation 87
6.3 Parameterization of the ADC 94
6.4 Summary and Conclusions 99

7 Conclusions and Future Work **101**

A Derivation of the Mean Squared Error **107**

List of Abbreviations **109**

List of Symbols **111**

List of Figures **115**

List of Tables **117**

Bibliography **119**

Publications and Patent **125**

1 Introduction

1.1 Motivation and Background

The technology of integrated circuits (ICs) experienced a rapid development in the last 20 years. Today, they are the basic building blocks for any kind of digital system and a life without ICs can not longer be imagined. In modern communications systems, they are substantial for data processing, e.g., digital signal processing for data transmission and reception. But for exchanging data between multiple devices, the digital signal (discrete amplitude and time) needs to be converted to a natural analog signal (continuous amplitude and time) and vice versa. The analog-to-digital converter (ADC) or digital-to-analog converter (DAC) provides this functionality and it is a key component in every radio transceiver. In practice, multiple topologies to implement an ADC exist. Depending on the required signal bandwidth and quantization resolution, another topology is suited best for the application. An overview of topologies and their operating ranges are given in Fig. 1.1.

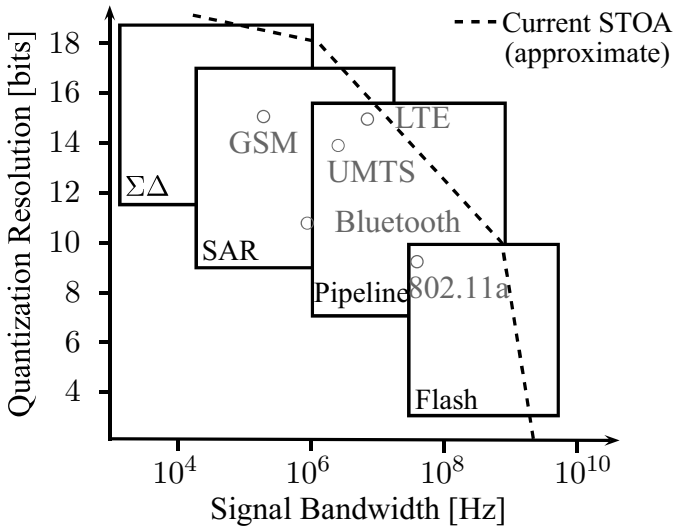


Fig. 1.1. Operating ranges of various ADC topologies and requirements for various cellular communication standards (○) (see [Rap+05], [HS11, Fig. 6.5]). In addition, an approximate on the current state-of-the-art (STOA) ADC technology is given.

The first radio transceivers have been tailored solutions to transmit and receive using a single data transmission band only. In these days, the number of new bands, modes and services is ever increasing. Hence, the amount of distinct built-in radio units per device also increases steadily. This again leads to an increased physical volume of the complete radio, e.g., in the handset. Usually, the rate at which new services are introduced is faster than the miniaturization of the packaging. Moreover, the printed circuit board area inside of a handset has become the second most precious and contested real estate in mobile communications directly behind the radio spectrum [CB13]. Hence, new concepts for a universal radio platform are necessary. The demand is on programmable radios, which enable transmission and reception of signals at any bandwidth, frequency band and any type of modulation. For this, Mitola envisaged the concept of an ideal software defined radio (SDR) [Mit95]. Applying this principle in a practicable radio receiver would cause extraordinary requirements in terms of the sampling rate and the quantization resolution to ensure reliable communications. Furthermore, the power consumption of such a device might exceed hundreds of watts. This kind of receiver will remain impracticable in the near future. Hence, a feasible ADC design needs to trade-off the three fundamental performance parameters [Luo11]: sampling rate, quantization resolution and power dissipation as shown in Fig. 1.2.

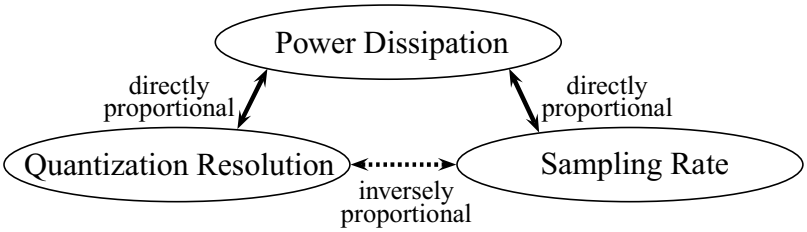


Fig. 1.2. Trade-off between the three fundamental performance parameters in analog-to-digital converters (ADCs) (see [Luo11]).

Mitola's visionary approach has to be softened for a more realistic design. Current advances in receiver design consider the development of a receiver which is capable of the reception of a single band situated at any frequency. The appropriate receiver concept therefore employs electronically tunable components [Abi07]. A tailored design of the receiver, when looking at the typical use of civilian mobile communication systems, foresees that a maximum of three to four communication channels are used at the same time. For example, when using a Bluetooth headset during a phone call and doing web search in parallel (*multi-mode*). Another scenario is carrier

aggregation in modern cellular standards, i.e., Long-Term Evolution (LTE). Here, multiple contiguous or non-contiguous frequency bands are aggregate to increased data throughput (*multi-band*). Hence, upcoming transceiver concepts need to be revisited carefully regarding their functional split of analog and digital processing to keep the receiver concept feasible. In this regard, a key towards the design of novel receiver concepts is the understanding of the ADC and its capabilities in bandpass signal conversion and multi-band/multi-mode signal processing.

1.2 Scope of the Thesis

The specifications of a suitable configuration of the bandpass sampling ADC for an application scenario is most often based on the analog circuit designer's experience or on existing solutions. To date, there is no analytical approach to quantify the possible parameter sets of an ADC. In this thesis, we tackle this problem and present a framework to obtain feasible ADC configurations. It is based on a general block diagram of the ADC and evaluates valid configurations based on the optimization of multiple objective functions, e.g., the input-output signal-to-noise ratio (SNR) or the ADC noise figure. These measures are directly related to higher level performance measures of the overall system, e.g., bit error rates for given coding schemes.

The obtained framework models each component of the converter according to its basic functionality taken from system theory, i.e., additive, multiplicative, or linear filter functions. This approach yields an understanding of the basics in each processing step, allows the tuning of individual elements in the chain, and a derivation of the impact on the chosen objectives. Applying this framework for ADC design has further advantages. It enables us to determine valid ranges of the individual ADC parameters. Furthermore, it allows to analyze different sets of parameters and trade-off between possible configurations. The proposed framework simplifies the ADC design process by optimizing the configurable parameters according to the signal characteristics and used receiver elements directly. Furthermore, it can be used to design improved bandpass sampling receivers.

Another key limitation for wireless modems arises from the non-ideal behavior of individual analog components, e.g., mismatch between the I/Q-path (I/Q-imbalance), non-linear power amplifiers and clock signal generators

impaired by phase noise (PN). The latter is the reason for two important impairments [Fet+05] of the homodyne receiver, i.e., random phase deviations during down-conversion mixing and clock jitter during sampling. In this work, we propose a novel receiver architecture which suppresses both impairments with one another by design. For this, the down-conversion mixer and the sampling circuit are fed with the same clock signal, and techniques of bandpass sampling are applied to improve the overall performance of the receiver. This allows to build an improved homodyne receiver which compensates the analog (RF) distortions directly in analog domain.

Both, the ADC parameterization framework and the advanced homodyne receiver concept, are the main investigations of this work and will be presented in subsequent chapters.

1.3 Outline and Main Contributions

The remainder of this thesis is structured as follows.

- In Chapter 2, an overview on the considered communication system is given and the used receiver architectures are presented. Moreover, the prospects and the challenges of the direct-RF-signal sampling approach are discussed.

- Chapter 3 focuses on the analysis of the realistic sampling circuit of an ADC in detail. Here, the track-and-hold and the sample-and-hold circuit are studied and their impact on the signal-to-noise ratio (SNR) performance for bandpass sampling is shown. We have published these investigations in [AKF13; AF13].

- In Chapter 4, the analysis of the sampling circuit is extended by incorporating the effect of sampling jitter. This impairment is of major concern in systems which sample the bandpass signal directly. Typically, two types of jitter are distinguished by their source: clock jitter and aperture jitter originating from the non-ideal reference oscillator and thermal noise in the circuit switches, respectively. The impact of these two types of jitter on the different sampling circuit models is discussed and the predominate effect is extracted. This analysis builds on the work of [LÖ6] and extends it to bandpass sampling. We have published the results in [AF14b; AF14a].

- The insights into sampling jitter are then used in Chapter 5 for the development of a novel homodyne receiver concept, which inherently compensates the effects of random phase deviations during mixing and sampling jitter. By introducing correlation between the clock signal of the down-conversion mixer and the sampling circuit, the architecture can gain several decibels of SNR for classical cellular scenarios. We have published the results in [AF15].

- In Chapter 6, the results from Chapter 3, 4 and Chapter 5 are used to analyze the bandpass sampling ADC. This includes a performance analysis of the complete receiver chain for a given scenario and investigations on the main limitations of this receiver concept. Moreover, we propose a framework to find feasible configurations of the ADC parameters, i.e., sampling rate, quantization resolution and jitter standard deviation, for a predefined input-output SNR constraint.

- Finally in Chapter 7, the thesis is concluded and future work is proposed.

The chapters 3, 4 and 5 concentrate on specific topics. The related literature and the contributions of this work are given in each of the chapters.

2 An Overview of Modern Receiver Architectures

This chapter gives a brief overview of the basic concepts and objectives in radio receiver design and analog-to-digital conversion. Moreover, prospects and challenges of the direct-RF-sampling receiver, which is a potential candidate for future radio receivers, are discussed.

Today's modern wireless communications devices, e.g., smartphones, tablets, or notebooks, employ a multitude of different radio access technologies (RAT) to ensure seamless connectivity for a variety of communications scenarios. For example, the Global System for Mobile Communications (GSM), the Universal Mobile Telecommunications System (UMTS), and the LTE standard for cellular communications, Wireless Fidelity (Wi-Fi) and Bluetooth (BT) for local area communications, and Global Positioning System (GPS) used for positioning. The design of standard-compliant and energy-efficient radio transceivers which are capable of communicating at multiple frequency bands (*multi-band*) and across multiple standards (*multi-mode*) is one of the main challenges for next generation mobile handsets and base stations [HS11; Jon07]. Until today, devices typically use dedicated modems for each communication standard and reutilization of single built-in components is rarely used.

The basic structure of the physical layer of a flexible radio transceiver is shown in Fig. 2.1. It consists of five main parts: the antenna, the analog front-end (AFE), the ADC and the DAC, the digital front-end (DFE), and the baseband processing and front-end control. The shown transceiver is generally capable of signal transmission and reception. The contributions of this thesis are the analysis of the requirements of future radio receivers with strong focus on the configuration of the ADC.

At the first stage in Fig. 2.1, the receiver comprises a smart antenna which adapts its directivity and the gain characteristics according to the needs of the received radio frequency (RF) signal. The desired RF or bandpass (BP) signal at the antenna is typically characterized in frequency domain by its

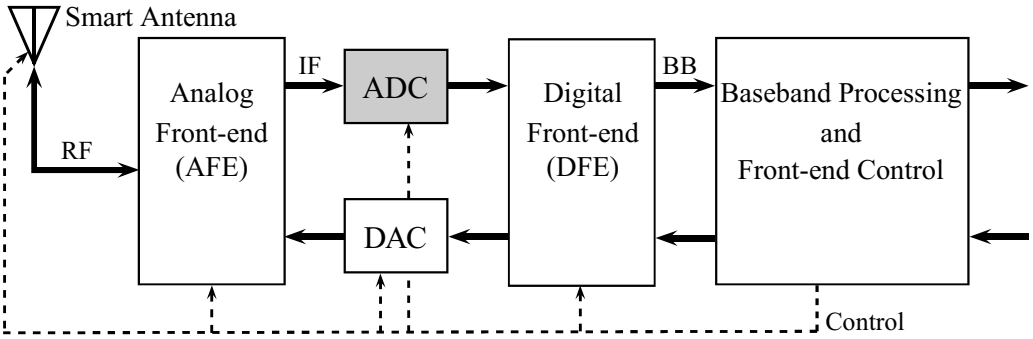


Fig. 2.1. Block diagram of a flexible radio transceiver (see [Ree02]).

center frequency f_c, the two-sided bandwidth $B = 2\,f_g$ and the power spectral density. The antenna output is then fed into the AFE. The AFE selects the desired signal bands, amplifies the signal with a low noise amplifier (LNA) and may already down-convert the signal to an intermediate frequency (IF) or to baseband depending on the receiver architecture. In the next step, the analog signal is digitized, that means it is converted from continuous-time and continuous-amplitude to a discrete-time and discrete-amplitude representation, using an ADC. If an IF signal is sampled with a certain sampling rate f_s, spectral replicas can occur close to baseband. Hence, the ADC carries out digitization and frequency translation simultaneously. This sampling technique is known as bandpass sampling [VSW91] or sub-sampling, and it is used in some state-of-the-art RF transceiver designs [HS11]. A general goal during the design of practical radios is that the desired signal is digitized as early as possible in the receive path while keeping it as long as possible digital in the transmit path. This allows to change the receivers operating parameters to accommodate new features and capabilities during runtime. After digitization, the DFE adapts the signal according to the requirements of subsequent baseband processing units. This includes channel selection of the signal bands, which is followed by an additional digital down-conversion, and sampling rate conversion [Hen01]. This flexible radio can be adapted according to the desired input signals, and the requirements for a reliable baseband processing by tuning the individual parameters of the available components.

While moving forward towards energy-efficient wireless radios for next generation cellular systems, the following general challenges (see [GM95]) need to be addressed: higher level of integration, lower power dissipation, smaller form factor, and lower production costs. This leads directly to the following research directions [HS11, p.282 ff.] in the design of radio receivers:

1. Reducing the amount of analog off-chip components, e.g., surface acoustic wave (SAW) filters, and switchable filter modules using microelectromechanical systems (MEMS).

2. Utilization of tunable on-chip RF filters enabling a flexible selection of the desired signal and advanced interference cancellation concepts.

3. Employing high dynamic range (DR) RF-ADCs to enable digitization of large signal bandwidths and a high sensitivity of the AFE.

4. Efficient algorithms for digital signal processing, e.g., channel selection, sample rate conversion and algorithms to compensate for non-ideal behavior of the AFE. The latter is of major concern as the cost-efficiency issue in current radio designs limits the quality and the performance of the entire system.

An approach towards a multi-band/multi-mode receiver is given by the concept of using basic digital building blocks [Abi07]. These building blocks are basic signal processing components, which can be programmed and connected such that they mimic the traditional analog structures. Given the large amount of different RATs, building blocks can reduce the necessary area for integration and production costs [Ako+99]. At the same time, the energy consumption of the radio can be reduced if the smart selection of the wireless air interface is applied [PFW11]. To ensure flexibility of the front-end for multi-band/multi-mode signaling, each component of the transceiver chain, e.g., filter, amplifier, mixer, sampler, and ADC, has to be selected carefully with respect to the requirements of the communication standard.

In the literature, two approaches for multi-band/multi-mode radios, or simply multi-band radios, are proposed [HS11].

1. The concept of using multiple independent receivers with tunable components, e.g., tunable down-conversion mixers with a variable oscillator frequency, adaptive filters, and adjustable LNAs. This concept is mostly based on the homodyne or the superheterodyne receiver architectures, which is discussed in Section 2.1.

2. The concept of using a single wideband receiver with early stage analog-to-digital conversion. This concept uses only a single analog path, but

has to cope with multiple distinct receive signals at the same time. For this, an increased sampling rate f_s, higher quantization resolution b and advanced digital post-processing algorithms are required. Channel selection of the multi-band signal is done in digital domain only. This concept is also known as direct-RF-sampling receiver (DSR) and is described in Section 2.2.

In the following, the working principles of the two receivers and the basics of the ADC are presented in Section 2.1, 2.2 and 2.3. Finally, we discuss the opportunities and the challenges of the direct-RF-sampling receiver (DSR) as a potential candidate for future radio receivers in Section 2.4. For this purpose, we have chosen a Wi-Fi scenario as the running example of this thesis. The explanations within this chapter build up the basis for the in-depth investigations of the analog-to-digital converter (ADC) and the direct-RF-sampling receiver (DSR) for the case of bandpass signal reception in the next chapters.

2.1 Two Conventional Receiver Architectures: Homodyne and Superheterodyne Receivers

The two most common architectures for an analog radio front-end are the homodyne and superheterodyne receiver. Their architectures, the operating principles, and their opportunities and limitations are discussed in the following.

2.1.1 Homodyne Receiver

The homodyne receiver shifts the desired bandpass (BP) signal with carrier frequency f_c to an IF band or into baseband using a single down-conversion mixer. The mixer performs a multiplication of the BP signal with a single-frequency wave at frequency f_{LO}, which is typically generated by the local oscillator (LO). Direct translation to baseband is ensured if the carrier frequency matches the frequency of the LO, $f_c = f_{\mathrm{LO}}$. The general structure of the homodyne receiver, which is also known as IF, low-IF, zero-IF or direct conversion receiver, is shown in Fig. 2.2.

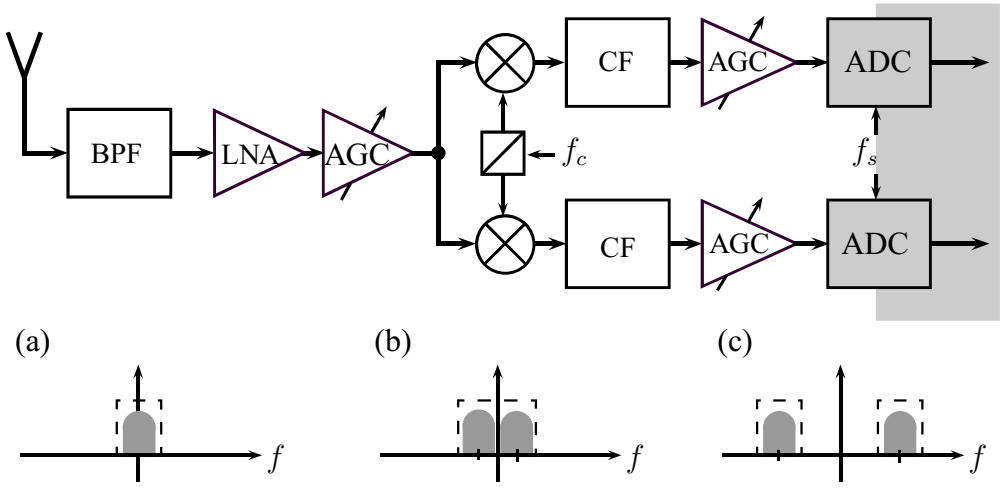


Fig. 2.2. Block diagram of the homodyne receiver. Moreover, the three common types of homodyne receivers: (a) direct-conversion, (b) low-IF and (c) IF are shown. The differences between the three receiver types is given by their individual frequency domain representation of the down-converted signal (gray shape) and the corresponding channel filter (CF) (dashed-line). Here, (a) only applies lowpass filtering whereas (b) uses a lowpass and a notch filter. In (c), a bandpass filter is used as the channel filter.

It employs filtering and amplifications of the BP signal by means of a bandpass filter (BPF), low noise amplifier (LNA), and automatic gain control (AGC), first. In a second step, the signal is transferred to an IF band or to baseband by the complex down-conversion mixer at frequency f_c. Then again, unwanted signal images and interferers are filtered by the CF, and the signal is scaled to analog-to-digital converter (ADC) input, accordingly.

For the *zero-IF receiver*, the sampling rate f_s of the ADC has to fulfill the Nyquist criterion $f_s \geq 2f_g$ and is typically chosen much smaller than the carrier frequency $f_s \ll f_c$. The receiver is called *low-IF receiver* if the ADC input signal is situated at a low IF frequency after down-conversion mixing. For this type of receiver, the sampling rate is chosen typically twice as high as the highest frequency of the IF signal $f_s \geq 2f_u$.

The advantage of the homodyne receiver is its reduced complexity and the low power consumption of the AFE due to the little amount of analog components, when comparing it to the superheterodyne receiver. Hence, it is a suitable radio receiver architecture used in many portable devices.

However, there are also many problems that arise when using this receiver architecture. One problem is due to the quality of the clock signal for down-conversion, which is typically generated by a LO using a phase-locked

loop (PLL). A low quality clock signal can distort the receive signal. Hence, the clock signal needs to fulfill certain requirements, e.g., limited amount of carrier frequency offset (CFO) and a small amount of PN, to ensure synchronous detection and proper baseband signal processing. Among all the other problems in homodyne receiver, e.g., I/Q imbalance or even-order distortions, LO self-mixing and self-mixing of strong interferers are of major concern [Raz97, Sec. 5.2.2]. All three introduce a direct current (DC) offset, can corrupt the signal itself and saturate the following stages. Hence, the DC offset limits the performance of the receiver. To cope with the DC offset, digital offset removal by a feedback path can be applied. Consider [Abi95; Raz97] for further reading about the zero-IF and low-IF receiver.

2.1.2 Superheterodyne Receiver

The superheterodyne receiver extends the concept of the homodyne receiver by using multiple down-conversion stages instead of just a single stage. Hence, the BP signal is translated to an IF, first, and then translated to baseband in subsequent stages. The superheterodyne receiver became popular due to its high selectivity and sensitivity, while keeping the requirements of single components low and the fabrication simple. But its large amount of off-chip components have become a major limitation for miniature and low power receiver design. That is the reason for leaving out the receiver block diagram and detailed explanations here. For further reading about this architecture consider [RW01].

2.1.3 Considerations on Flexibility and Basic Limitations

Current and upcoming wireless communication standards require new developments in the receiver architecture. Currently, researchers focus their investigations on two properties:

- reconfigurable architectures that allow frequency and standard independent signal reception (multi-mode), and

- architectures for parallel reception of multiple frequency bands (multi-band) at the same time .

Both properties, multi-mode and multi-band, can be implemented by using either independent receiver chains for each signal band or a single wideband analog front-end as discussed earlier in this chapter. This means that the receiver chains either use independent resources or share a set of functional building blocks. The latter gives the opportunity that complexity and power consumption of the analog front-end is independent of the number of receive bands.

In order to realize the frequency agility and standard independence, it is necessary to introduce tunable and interchangeable components in each of the receive chains. Basic building blocks for an adaptive receiver are variable filters, multi-band LNAs, programmable ADCs, and mixers including tunable oscillators. Typically, each of these building blocks has to trade-off different objectives. The LNA and the mixer need to balance power consumption and dynamic range, whereas the oscillator trades power consumption against its intrinsic frequency and the phase noise properties. Moreover, implementing various building blocks for multi-mode operation increases the liability to hardware impairments [Sch08], i.e., non-linear amplification, PN, I/Q imbalance, and sampling jitter. In this case, digital estimation and compensation methods may have to be applied to ensure proper performance [Fet+05]. According to [HS11, Chapter 3], the topology of a fully adaptive multi-mode/multi-band receiver consists of three basic parts: the adaptive AFE (including BPF, LNA, mixer, LO), the adaptive analog baseband (lowpass filter (LPF), AGC), and the adaptive digital back-end (ADC, DFE).

The concept of functional building blocks offers great potential for low power consumption, small die area, and may reduce the overall costs due to the reduction of the number of analog components, reusing existing parts, and make use of large scale silicon integration. The aim of a tunable receiver is to ensure a certain performance according to the different requirements of each standard, e.g., sensitivity, frequency masks, and SNR requirements, at low power operation.

2.2 Direct-RF-Sampling Receiver Architectures

A modern approach in the design of radio receivers is pushing the digital signal processing closer to the antenna [Ree02]. The objective is to reduce the complexity of the analog front-end (AFE) by means of an advanced digital processing. In 1995, Mitola presented his vision of the ideal software radio architecture [Mit95], which samples the BP signals directly at the antenna. The main difference between the DSR and the homodyne receiver concept is the down-conversion stage. Here, the DSR uses a sampling circuit instead of an analog down-conversion mixer as shown in [Kes95]. This concept allows on-chip processing at an early stage of the receiver chain and reduces the amount of analog off-chip components. Moreover, it provides a flexibility receiver chain to receive signals with different carrier frequencies and bandwidths [Abi07]. A basic model of the direct-RF-sampling receiver (DSR) is shown in Fig. 2.3.

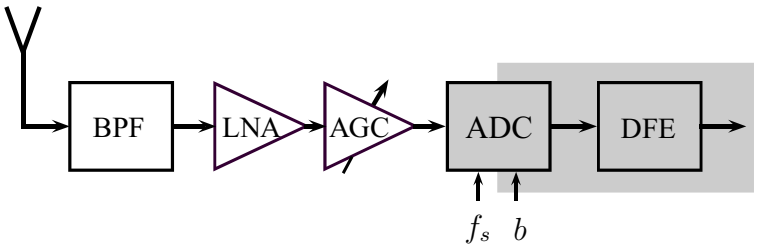


Fig. 2.3. Block diagram of the direct-RF-sampling receiver (DSR) according to Mitola's vision.

First, the received BP signal is bandpass filtered and amplified like in a homodyne receiver. Afterwards, the RF signal is directly digitized by the analog-to-digital converter (ADC). The reduced amount of components in the AFE has the drawback of increased requirements on each of the remaining components. Especially the ADC has to provide a much higher sampling rate f_s and a higher quantization resolution b to handle the tremendous dynamic range and bandwidth of the received wideband signal. High sampling rates and high quantization resolutions implicate an increased power consumption of such a receiver. Hence, a proper configuration of the receiver has to account for the dissipated power.

An approach to obtain moderate sampling rates is given by applying BP sampling which is also known as sub-sampling. For this purpose, the sampling

rate is chosen below the lowest BP signal frequency $f_s < f_l$. The classical theorem for uniform sampling of BP signals (see [VSW91]) states that a signal can be perfectly reconstructed if the sampling rate is at least $f_s \geq 2f_u/k$, where k is the largest integer within f_u/B, denoted by $k = \lceil f_u/B \rceil$. Furthermore, a sub-sampling factor is defined as the ratio of Nyquist sampling rate ($k = 1$) to sub-sampling rate ($k \geq 1$) for BP sampling: $F_\mathrm{s} = f_{s,\mathrm{NYQ}}/f_{s,\mathrm{BP}} \geq 1$.

Now, let us consider a continuous-time input signal $x(t)$ sampled at a rate $f_s = 1/T_s$. The corresponding output signal $x_\mathrm{s}(t)$ can be written as

$$x_\mathrm{s}(t) = x(t) \cdot \Delta_{T_s}(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta\left(t - n\,T_s\right). \tag{2.1}$$

The function $\Delta_{T_s}(t)$ is the Dirac-comb function also known as the sampling function. The corresponding Fourier transform $X_\mathrm{s}(f) = \mathcal{F}\{x_\mathrm{s}(t)\}$ is given as

$$X_\mathrm{s}(f) = \left(X * \Delta_{\frac{1}{T_s}}\right)(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X\left(f - n\,f_s\right). \tag{2.2}$$

Here, the $*$-operator denotes the convolution.

In the DSR, sampling is typically used for the discretization in time and for down-conversion of the RF signal from a higher Nyquist zone to an intermediate frequency in the first Nyquist zone $[0, f_s/2)$. Hence, BP sampling uses the aliasing property to inherently down-convert the received BP signals. In order to avoid aliasing between different BP signals or self-aliasing, the sampling rate f_s has to be chosen with respect to the carrier frequencies and bandwidths of all received signals.

Now, consider a bandlimited input signal $x(t)$, which is located in the frequency range (f_l, f_u) with the bandwidth $B = f_u - f_l$, and the lowest signal frequency $f_l = f_c - B/2$ and the highest signal frequency $f_u = f_c + B/2$. This BP signal $x(t)$ has to be sampled at the following rate f_s to ensure aliasing-free signal reception (see [VSW91]):

$$\frac{2f_u}{k} \leq f_s \leq \frac{2f_l}{k-1}, \quad \forall k : k = \left[1, \frac{f_u}{B}\right] \in \mathbb{Z}. \tag{2.3}$$

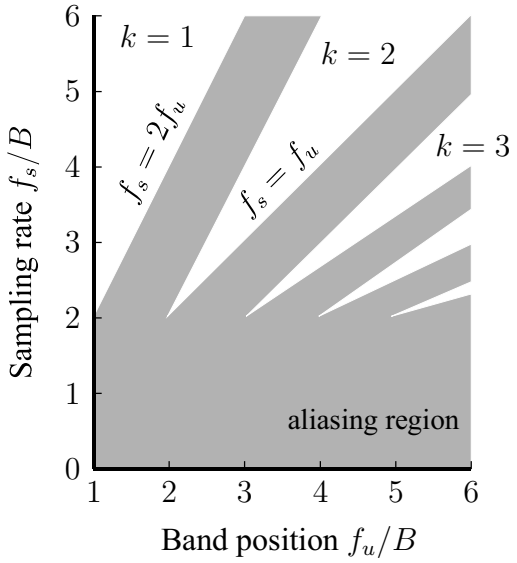


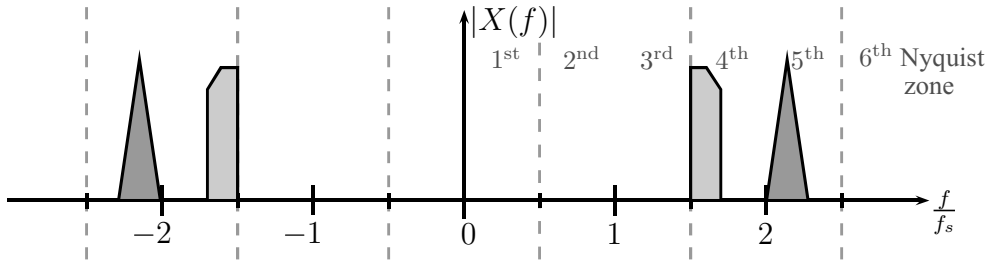
Fig. 2.4. Possible sampling rates f_s for aliasing-free sampling of bandpass (BP) signals (white regions) in the frequency range (f_l, f_u), the bandwidth $B = f_u - f_l$, and the region where aliasing occurs (gray region) according to (2.3).

The sampling rates that follow from (2.3) are shown in Fig. 2.4. The lowest possible sampling rate $f_s = 2\,B$ can be achieved for integer ratios of the band position f_u/B and is only important from a theoretical viewpoint. Practical systems will most likely require a higher sampling rate to cope with slight deviations of the assumed frequencies and other design imperfections. In addition, guard bands may be introduced to reduce the sensitivity to small changes in frequency and to protect against aliasing [Oya+12].

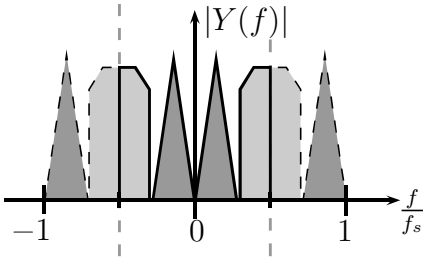
Moreover, the DSR architecture offers the potential of parallel reception of multiple independent signal bands by a single analog front-end (AFE). For this, the band positions have to be known a priori. The concept of multi-band signal reception is shown in Fig. 2.5.

The two BP signals are translated from the fourth and the fifth Nyquist zone (NZ) to the first NZ $[0, f_s/2)$. In this example, the sampling rate is chosen such that no aliasing occurs. An algorithm to determine the feasible sampling rates for different setups has been proposed in [Ako+99].

The ability of receiving multiple signal bands at the same time is one of the major advantages of the DSR, but it is also the major drawback of the architecture. The reason is the following. Both, interference and noise components may fold into the desired signal band due to sampling and hence degrade the SNR in the band-of-interest. The reduced SNR implicates a performance degradation. The effect of noise and interference folding, and the



(a) Spectrum of the input signal prior to sampling.



(b) Spectrum after sampling at the rate f_s.

Fig. 2.5. (a) Magnitude spectrum $|X(f)|$ of a multi-band input signal $x(t)$ before sampling and (b) magnitude spectrum $|Y(f)|$ after sampling with a sampling rate f_s at the output.

interaction with realistic sampling circuits will be touched in more detail in Chapter 3.

Another drawback of the DSR is its vulnerability to non-ideal sampling times which arise due to a non-ideal sampling clock signal, i.e., local oscillator (LO) signal of the sampling clock will be impaired by phase noise (PN), and thermal noise in the circuit switches. The introduced sampling time errors, also known as sampling jitter, translate to amplitude errors and hence limit the system performance further. Sampling jitter is of major concern for BP sampling because its intensity is directly proportional to signal frequencies [Wal99]. In Chapter 4, the impact of the different types of jitter on the characteristics and the SNR performance of a realistic sampling circuit is studied. It extends the basic work of [LÖ6] towards sampling of BP signals and includes the concepts of the work of [Syr12], regarding the analysis of oscillator impairments.

The performance of a DSR in a realistic environment will strongly rely on the available dynamic range (DR)[1] of the AFE. The architecture drawbacks, i.e., the susceptibility to interference and noise folding, sampling jitter, and

[1]The dynamic range (DR) describes the ratio of the maximum power level of the input signal to its minimum detectable value. An exemplary calculation of the available dynamic range is presented in Section 2.4.

also a limited quantization resolution, reduce the available DR and need to be considered. The interference and the noise power can be reduced by improving the band-selection capabilities of the receiver before quantization.

For this purpose, the concept of discrete-time (DT) signal processing after the sampling stage has been introduced [GT86]. DT processing offers the potential to design filters, amplifiers, and decimation units using standard semiconductor process technologies, e.g., switched-capacitor circuits. The signal itself is represented in discrete-time and continuous-magnitude. Merging the concept of DT processing into the ideal DSR from Fig. 2.3 has led to a new promising receiver architecture, the discrete-time direct-RF-sampling receiver (DT-DSR). The basic structure of the DT-DSR is shown in Fig. 2.6.

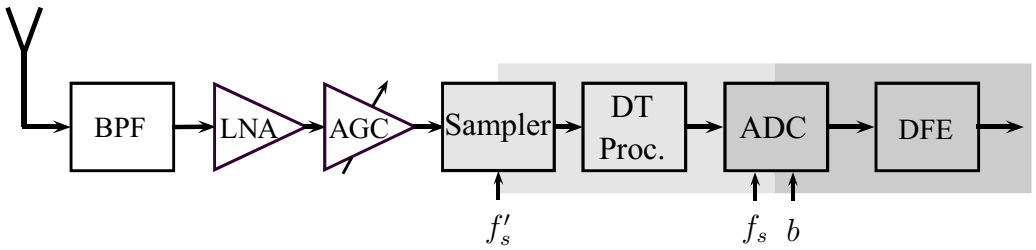


Fig. 2.6. Block diagram of the discrete-time direct-RF-sampling receiver (DT-DSR) with enhanced discrete-time (DT) signal processing.

The DT-DSR combines the advantages of an early stage digitization and on-chip processing of the DSR with the band-selection capabilities of the homodyne receiver. Hence, low power and flexible receivers can be realized, see e.g., the first RF front-end using integrated DT filtering by [SLW96] and an integrated single-chip solution for Bluetooth and GSM by [MSL05]. Moreover, it has been shown that clever analog design and architectures in a digital technology achieve the performance that is equivalent to a dedicated radio [Cra12]. Most favorable is the property that the sampled receive signal with its continuous-amplitude is much better conditioned to ADC input. This means that the interference is filtered and the dynamic range of the overall signal is decreased. Moreover, the initial sampling rate f_s' can be reduced to f_s by decimation. This again reduces the dissipated power of the used ADC and makes the DT-DSR a feasible architecture. Still, the DT-DSR does not account for noise aliasing suppression similar to the DSR.

Even after introducing the DT-DSR, it is reasonable to state that Mitola's ideal direct-RF-sampling architecture is hardly feasible for fully flexible and

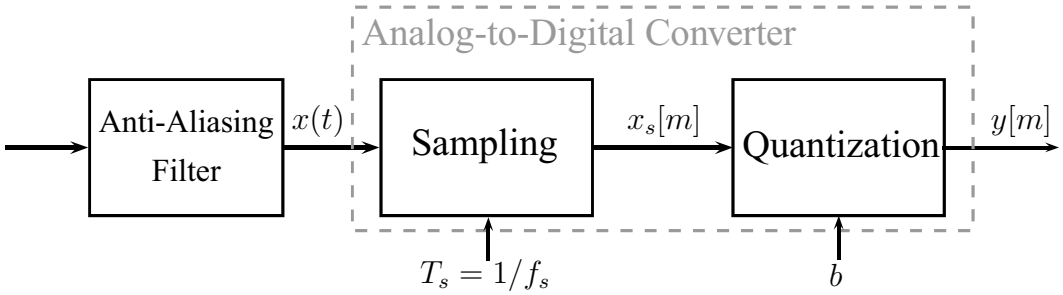
wideband signal reception due to its limitations in the available dynamic range. The extension of the ideal DSR by means of DT signal processing is a promising solution to circumvent the most limiting problems, and still retain most of the flexibility of the DSR concept. The key towards the all-digital receiver structure is to widen the view of the analog-to-digital conversion process by introducing the DT processing stage between the conventional sampling and quantization stage. More generally speaking, the DT-DSR is similar to the homodyne receiver, but employs a sampling circuit for signal down-conversion instead of a down-conversion mixer.

2.3 Analog-to-Digital Converters

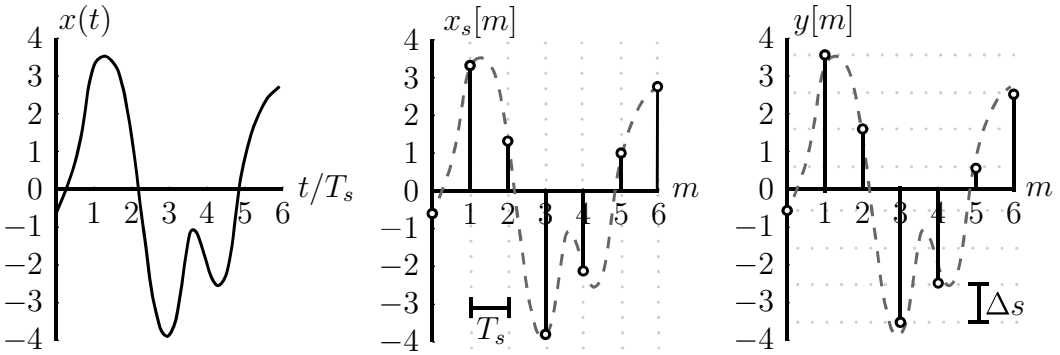
The main purpose of an analog-to-digital converter (ADC) is the conversion of an analog signal, which is continuous in time and amplitude, to a digital signal, which is discrete in time and amplitude. The ADC is a key element in digital radio receivers and it is of particular importance when applying BP sampling. In this case, the anti-aliasing filter prior to the bandpass sampling ADC (BP-ADC) is not solely a lowpass filter in the frequency range $[0, f_s/2]$. It is a BP filter and may need to be adapted to the band position of the desired input. Furthermore, BP anti-aliasing filtering is not necessarily limited to a single frequency band, i.e., multi-band reception requires a bank of BP filters [TC06].

The ADC comprises two basic consecutive stages: sampling and quantization. In Fig. 2.7, the block diagram of an ADC and the time-domain representation of a converted signal is shown. First, the sampling stage, to discretize the signal in time at rate $f_s = 1/T_s$, and second, the quantization with a resolution of b bits or 2^b output levels to discretize the amplitude. Here, the quantization step size is denoted as Δs.

The sampling stage follows the explanations given in Section 2.2 before. The second integral part of the analog-to-digital conversion is the discretization of the amplitude by a finite set of output values. The mapping of a continuous amplitude to a discrete and finite set of outputs is inevitable related to amplitude errors. These quantization errors limit the performance of the ADC and need to be considered carefully. The process of quantization, which is a non-linear operation in its nature, can be described using Widrow's model published in [WK96]. The approach allows to replace the



(a) Basic block diagram of an ADC with an anti-aliasing filtering.



(b) Time-domain signal at each stage of the ADC.

Fig. 2.7. Basic structure and functionality of an ADC.

quantizer, given a fine grained quantization, by an additive noise source. This noise is called pseudo quantization noise (PQN) and will be described in the Section 2.3.2.

2.3.1 ADC Topologies and Figure-of-Merits

In a practical system setup, several types of ADC topologies are available. Each has its benefits and drawbacks, and needs to be selected depending on the intended application. Commonly used topologies are the $\Sigma\Delta$-ADC, Flash-ADC, successive approximation register ADC, and the time-interleaved ADC. A comprehensive overview on existing architectures is given by [Le+05]. A summary on basic design principles can be found in [Raz95; Raz97] and [Kes05], respectively. Advances in the ADC design, e.g., high dynamic range ADCs and low power solutions, drive the development towards a real software radio.

The appropriate ADC topology for a given application is typically chosen according to the following requirements:

- sampling rate f_s,

- nominal quantization resolution of b bits, where 2^b gives the number quantization levels, or the effective number of bits (ENOB)[2],
- analog input bandwidth or 3 dB cutoff frequency of the sampling circuit $f_{3\mathrm{dB}}$,
- power consumption P_{ADC} of the ADC.

A consistent figure-of-merit (FOM) was defined in [Wal99] to compare the performance of ADCs. The Walden-FOM is defined as

$$\mathrm{FOM} = \frac{2^{\mathrm{ENOB}} \cdot f_s}{P_{\mathrm{ADC}}}, \tag{2.4}$$

and relates the ADC performance, by using the product of quantization levels and sampling rate, to the dissipated power P_{ADC}. Applying BP sampling techniques implies lower sampling rates and hence less dissipated power [Pos13] under certain conditions. Thus, the FOM can be improved when using BP-ADCs.

An extensive survey about existing ADCs and their FOMs is given by [Mur]. Moreover, projections for the future ADC designs are given by [Jon13]. Both show that the improvements in the achievable sampling rate or quantization resolution under certain power constraints are tied to the ADC topology. Most of the published ADCs in these surveys have a high quantization resolution and only very few minimize the FOM for high sampling rates and low quantization resolution. As a general rule of thumb, the Walden-FOM improves by factor two every 2.5 years for $\Sigma\Delta$-ADC, and it improves by factor two every 1.8 years for Flash-ADCs. This corresponds to an FOM improvement by a factor of 4 for $\Sigma\Delta$-ADC and a factor of 6.9 for Flash-ADC every five years. Furthermore, [Jon13] projects the Walden-FOM to be 0.2 fJ per conversion step in the year 2020. Until now, most of predictions on the performance and power consumption are made empirically. In [SMS09], analytical bounds of the power dissipation of high-speed Nyquist-ADCs are studied, first. It was found that the power dissipation of high quantization resolution ADCs is limited by the thermal noise, whereas the process technology is the limiting factor for the case of low-resolution.

[2] ENOB specifies the quantization resolution of an ideal ADC that already considers the limitations of a real ADC, e.g., circuit noise and further distortions. It is a measure for the dynamic range (DR) of an ADC. The value of the ENOB is typically smaller than the nominal resolution $\mathrm{ENOB} < b$.

Note that we consider frequency ranges of the received signal in the lower gigahertz regime from 1 - 10 GHz in this work. For this range, the transit frequencies f_{T} of the switching circuits are considered to be sufficiently high such that the comparator ambiguity [Wal99] is not limiting the overall signal quality. Moreover, we assume linear quantization with uniform steps size Δs in a given range of the amplitude and no further impairments of the quantizer, e.g., integrated or differential non-linearity (INL/DNL) errors.

2.3.2 Pseudo Quantization Noise Model

According to the work of [WK96],[WK08, Ch. 5] and [Ree02, Ch. 5], the quantization error can be modeled as an additive white Gaussian noise (AWGN) term $n_{\mathrm{q}}(t)$. This approximation is based on Bussgang's theorem [Bus52]. The pseudo quantization noise (PQN) has a total noise power $P_{\mathrm{q}} = \Delta s^2/12$, which only depends on the quantization step size Δs assuming a uniformly distributed amplitude of the error signal. By applying the PQN model, the quantized output signal $y[m]$ can be written as the sum of the sampled input signal $x_{\mathrm{s}}[m]$ and the additive quantization error $n_{\mathrm{q}}[m]$:

$$y[m] = x_{\mathrm{s}}[m] + n_{\mathrm{q}}[m]. \tag{2.5}$$

In Fig. 2.8, the power spectral density (PSD) function of the quantized signal $S_y(f)$, located at the carrier frequency $f_c = f_s/4$ with the bandwidth $B = f_s/8$, is shown. Furthermore, the PSD of the error signal $S_{n_{\mathrm{q}}}(f)$ for low to medium quantization resolution is given. It can be observed that the error spectrum changes from a colored spectrum for 1 bit to an almost white spectrum for 5 bits or 6 bits. Hence, the PQN approximation can be used to describe the variance of the quantization error for medium to high quantization resolutions of more than 6 bits. Furthermore, it is useful to describe the performance of the ADC.

The performance of the quantizer is commonly described by the metric of the signal-to-quantization-noise ratio (SQNR). The SQNR γ_{Q} is defined as the ratio of the average input signal power $P_{x_{\mathrm{s}}}$ to the quantization noise power P_{q}:

$$\gamma_{\mathrm{Q}}\left(b, \eta\right) = \frac{P_{x_{\mathrm{s}}}}{P_{\mathrm{q}}} = \frac{3 \cdot 4^b}{\eta}. \tag{2.6}$$

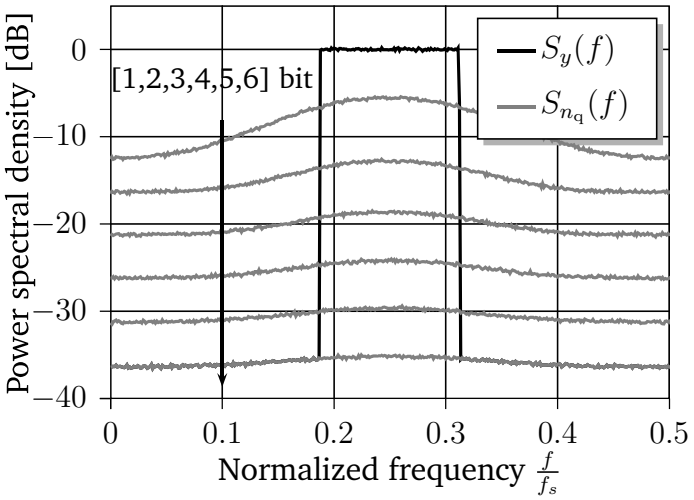


Fig. 2.8. Power spectral density of a quantized bandpass signal $S_y(f)$ (black) and the error signal S_{n_q} (gray) with $1, 2, \ldots, 6$ bits of resolution (from top to bottom).

The SQNR is also given as a function of the quantization resolution b and the peak-to-average-power ratio (PAPR) η of the input signal [Ree02, Eq. (5.27)]. The quantity of the PAPR η is of interested, because most of the received signals show high peak power values as compared to their average power and high PAPR values limit the performance of the quantizer. The PAPR can be described by the ratio of the input signal's peak power to its average power: $\eta = \max\left\{|x_s|^2\right\} / E\left\{x_s^2\right\}$. Here, $E\{\cdot\}$ denotes the expectation operator.

Improvements on the SQNR of the digitized signal can be achieved if oversampling is applied. In this case, the sampling rate f_s is chosen higher than required Nyquist rate and additional filtering realized in digital domain. A higher sampling rate reduces the noise power density in the signal band, while keeping the overall quantization noise power constant, and a digital brickwall filter attenuates the out-of-band quantization noise. Oversampling is typically specified by the value of the oversampling ratio (OSR). We define the OSR β for a single ADC, e.g., for bandpass sampling, to be $\beta = \frac{f_s}{2 \cdot B}$, and for the homodyne receiver with two separate ADCs in the I- and Q- branch or quadrature sampling [Bro79] to be $\beta = \frac{f_s}{B}$. This yields to

$$\gamma_{\mathrm{Q}}(b, \eta, \beta) = \frac{3 \cdot 4^b}{\eta} \cdot \beta = [\,6.02\,b + 4.77 - 10\log_{10}\eta + 10\log_{10}\beta\,]\ \mathrm{dB}. \quad (2.7)$$

It can be observed that the SQNR increases by approximately 6 dB if the quantization resolution b is increased by one bit or the sampling rate is in-

creased by a factor of $\beta = 4$. Whereas the SQNR decreases if input signals with higher PAPRs η are digitized.

The presented equations for the SQNR will be used for further evaluations of the overall ADC model in all following chapters.

2.4 Prospects and Challenges of Direct-RF-Sampling Receivers

In the last decade, the concept of direct-RF-sampling has received an increased attention in the design of multi-mode/multi-band radio receivers. Several implementations have been reported, e.g., the fully integrated reconfigurable radio for GSM and Bluetooth [MSL05], and the multi-band direct-RF-sampling receiver front-end for Wi-Fi [And+07]. The reported receivers have shown the general feasibility of a direct-RF-sampling approach and they have paved the way for a novel receiver design methodology.

Now, let us consider an exemplary IEEE 802.11a Wi-Fi transmission scenario, which operates at carrier frequencies at around 5.6 GHz, has a bandwidth of 20 MHz per sub-band, and uses orthogonal frequency-division multiplexing (OFDM) with quadrature amplitude modulation (QAM). This example is considered as the running example during this thesis. The respective Wi-Fi signal shall be received by a DSR as shown in Fig. 2.3. For this purpose, the sampling rate f_s and the quantization resolution b have to be chosen such that the resulting SNR after digitization still allows reliable communications. Successful baseband processing is ensured given that the following two requirements are fulfilled. First, the *sampling rate* f_s is chosen such that no self-aliasing (see Fig. 2.4), and aliasing due interference or noise occurs. Second, the *quantization resolution* b complies with the dynamic range requirements of the input signals to limit the SQNR losses. Moreover, sampling rate and quantization resolution have to be balanced carefully to keep the overall power consumption of the receiver at a moderate level.

In our example, the analog bandpass filtering stage from Fig. 2.3 selects the complete industrial, scientific and medical (ISM) transmission band from 5.5 - 5.7 GHz, and suppresses most of the unwanted out-of-band interference. The subsequent amplifiers adapt the filtered input signal to the requirements of the BP-ADC. The amplified band is then sampled using the minimum

Parameter	Description
$\mathrm{DR_Q}$	Quantization noise back off
$\mathrm{DR_{SIG}}$	SNR of the received signal, its PAPR, and contingent fading margins due to the transmission channel
$\mathrm{DR_{ACI}}$	Margin for in-band interference from adjacent channels
$\mathrm{DR_{AFE}}$	Degradations due to bandpass sampling approach, e.g., folding of interference and noise, and losses due to realistic sampling circuits
$\mathrm{DR_{IMP}}$	Additional margin for non-ideal behavior of the AFE, e.g., nonlinear amplification, and sampling jitter

Tab. 2.1. Main dependencies of the ADC operating range.

possible sampling rate of 407.14 MHz $\leq f_{s,\min} \leq 407.4$ MHz for aliasing-free reception, which has been derived from (2.3). For the calculated sampling rate $f_{s,\min}$, the resulting spectral image in the first Nyquist zone appears as a mirror image of the original band. Mirror images can be prevented by using a slightly higher sampling rate in the range of 422.22 MHz $\leq f_{s,\min} \leq 423.07$ MHz. For the second sampling rate, the original signal band is located in an odd Nyquist zone instead of an even Nyquist zone (see example in Fig. 2.5).

An estimate on the required quantization resolution b can be obtained from the dynamic range (DR) requirements of the desired input. Matching the required DR with the available resolution of the quantizer ensures that strong and also weak signals are detectable in the presence of strong in-band interference. The required DR, also known as the ADC operating range [Ree02], typically depends on the parameters given in Table 2.1.

All these values sum up to the total required dynamic range DR as

$$\mathrm{DR} = \mathrm{DR_Q} + \mathrm{DR_{SIG}} + \mathrm{DR_{ACI}} + \mathrm{DR_{AFE}} + \mathrm{DR_{IMP}}. \tag{2.8}$$

In Fig. 2.9, an example for the ADC operating range is given for the two bandpass sampling receivers: the DSR and the DT-DSR. It follows the structure of (2.8). Both receivers have similar requirements on the DR originating from the input signal $\mathrm{DR_{SIG}}$ and the quantization noise back off $\mathrm{DR_Q}$. The largest portion of the DR budget of the ideal DSR (left) is the in-band in-

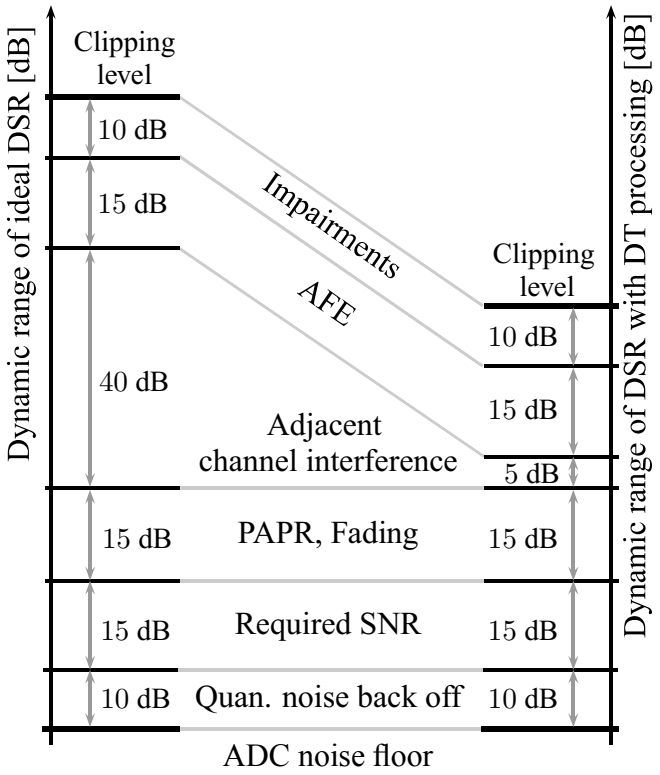


Fig. 2.9. Exemplary comparison of the dynamic range (DR) requirements of the ADC from Table 2.1 for using the direct-RF-sampling receiver (DSR) (left) and the discrete-time direct-RF-sampling receiver (DT-DSR) (right).

terference with approximately 40 dB. This is due to the fact that there is no additional in-band filtering as compared to the DT-DSR or the homodyne receiver. For the ideal DSR concept, in-band filtering is done in the digital domain and hence the digitization stage has to cope with it. Moreover, direct bandpass sampling leads to increased distortions due to circuit impairments, and signal quality degradations due to the AFE. In total, this adds up to a required DR of about 105 dB, which corresponds to a quantization resolution of about 17 - 18 bits. An ADC with a sampling rate of $f_s \approx 423$ MHz and quantization resolution of $b = 18$ bits is generally not feasible in practice. Hence, the main challenge in the design of a fully digital receiver is to overcome the limitations of the ADCs dynamic range [Ree02, p. 13]. For this, the AFE has to smartly compromise the three key stages: band-selection, down-conversion, and analog-to-digital conversion.

A feasible approach to tackle the issue of a limited DR, e.g., due to large in-band interference, is given by the discrete-time direct-RF-sampling receiver (DT-DSR) which has been shown in Fig. 2.6. The DT processing, after sampling the bandpass signal, allows to condition the desired signal band such that its DR can be reduced dramatically. It down-converts the signal

by an initial sampling circuit operating at rate f_s'. Afterwards, strong out-of-band (OOB) and in-band interference is filtered and the signal is amplified. Moreover, the initial sampling rate f_s' can be significantly reduced to $f_s \ll f_s'$ by decimation. It can be seen in Fig. 2.9 that applying this technique can significantly reduce the impact of $\mathrm{DR}_{\mathrm{ACI}}$. Still, the remaining DR requirements are round about 70 dB, or 12 bits, but the sampling rate could be reduced close to its minimum $f_s \approx 2B$. The overall DR budget can be optimized further by a proper design of the AFE and the careful evaluation of its non-ideal behavior $\mathrm{DR}_{\mathrm{IMP}}$. However, the required signal quality and the quantization noise back off are fixed due to communication standard.

2.5 Summary

This chapter has laid the basics for the design of modern receiver architectures. For this, the traditional homodyne and superheterodyne receiver, and direct-RF-sampling receiver have been presented and their advantages and disadvantages have been discussed. Moreover, the analog-to-digital converter has been identified as a key element in the digital radio receiver in particular for bandpass sampling applications. Finally, the prospects and the challenges of the direct-RF-sampling receiver have been discussed by means of an exemplary Wi-Fi application scenario. Based on the evaluations of the ADC operating range, it was exemplary shown that the discrete-time direct-RF-sampling receiver (DT-DSR) is a feasible and promising candidate for a multi-mode/multi-band radio receiver.

In the next two chapters, we will continue our investigations on the basic limitations of the DSR. This includes the evaluation of the impact of realistic sampling circuits on the performance of the DSR in Chapter 3 and the evaluations of sampling jitter in Chapter 4. Furthermore, we give important design considerations for the sampling circuit of the direct-RF-sampling receiver to operate at moderate dynamic ranges.

3 Direct-RF-Sampling with Realistic Sampling Circuit Models

This chapter analyzes the concept of direct-RF-sampling in the light of realistic sampling circuits. For this, a system model is described and evaluated for the two common types of samplers: voltage and charge sampling. Finally, implications for the design of the direct-RF-sampling receiver (DSR) are discussed.

An ideal uniform sampler produces samples with equidistant time-spacing T_s and values equivalent to the instantaneous amplitude of the continuous-time (CT) signal. This can be modeled as a multiplication of the desired signal and the Dirac-comb function, which has been presented in (2.1), earlier. The ideal sampling model holds for the case of baseband or low-IF signal sampling, which is known as Nyquist sampling, where $f_s \geq 2\,f_g$ or $f_s \geq 2\,f_{\mathrm{u}}$. Here, f_g and f_{u} denote the one-sided bandwidth of the baseband signal and the highest frequency of the IF signal, respectively.

Moreover, the ideal sampling model can also be used to understand the basics of the bandpass sampling theory. Here, images of the original signal band are shifted by multiples of f_s and hence appear in the first Nyquist zone. These frequency-shifts are the basis of the DSR to skip the down-conversion mixer in the analog front-end (AFE). The theory of bandpass sampling has been investigated by Vaughan [VSW91], first. It is well aligned with the Nyquist theorem [Nyq28] stating that a minimal sampling rate $f_s \geq 2B$, for a single ADC and complex signals, or $f_s \geq B$, for quadrature sampling [Bro79], needs to be fulfilled. Aliasing is advantageous for the BP signal sampling, but residual interference and noise may also fold into the desired signal band and hence fundamentally degrade the achievable SNR performance [ME11]. This is the case given that noise is considered to be wideband with a bandwidth larger than the sampling rate. Consequently, the spectral components of the noise add up and the noise density increases. This effect is commonly known as noise folding and it decreases the SNR in the band-of-interest. The effect of noise folding is shown in Fig. 3.4b and a detailed analysis is given in Section 3.1.3.