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Sami Ur Rehman

Time-Domain Broadband Data Conversion Transceiver Circuits in CMOS

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TIME-DOMAIN BROADBAND DATA CONVERSION TRANSCEIVER CIRCUITS IN CMOS

Sami Ur Rehman

der Fakultät Elektrotechnik und Informationstechnik
der Technischen Universität Dresden

zur Erlangung des akademischen Grades

Doktoringenieur
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genehmigte Dissertation

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Dedicated to parents everywhere, who, unlike others, selflessly love and provide for us while giving one sacrifice after another.

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ABSTRACT

The advent of 5G technologies and Internet-of-Things (IoT) applications is pushing the annual information and communication growth rate upwards of 8%. Such a startling surge in the amount of information is putting power and performance limitations on each aspect of communication infrastructure. In the framework of hardware design, for both cellular as well as short-haul serial links, transceiver circuits are being developed to achieve highest possible energy efficiency. Transceiver circuits primarily consist of analog RF front end blocks and data converters, which convert the digital information into an analog waveform and vice versa. Conventionally, the data converter on the transmit-side of the link translates the digital data into the amplitude of an analog waveform. And the receive-side data converter simply decodes this amplitude information back into digital data. In scaled CMOS technologies, however, such amplitude-domain data converters suffer dynamic range degradation since they are forced to operate at lower supply voltages for device breakdown considerations, thereby deteriorating the noise figure of the entire link. To address this scaling-caused noise figure degradation issue, encoding the digital information in a time variable, instead of an amplitude variable, on the transmit-side, and subsequently, performing quantization in time domain on the receive-side is one promising option. This work presents several time-domain energy-efficient transmit- and receive-side data converters in 45-nm SOI CMOS node.

A unique high oversampling input-delayed delay-line based receive-side data converter is first presented. This highly scalable multi-standard adaptable data converter architecture digitizes transitions/threshold crossings and inter-transition distances inside any time-domain binary input symbol sequence. The circuit works by sampling delayed replicas of a threshold-crossing binary input symbol sequence inside a differential delay-line. The resulting sampled digital word carries information of the threshold-crossings and the distances between them. The delay-line data converter has been designed and demonstrated to oversample any time-domain analog waveform data with the best reported power efficiency of 1.62 pJ/bit. To minimize the jitter, the design of the delay-element, used inside the delay-line of the data converter, as a Bessel filter is detailed and mathematical models for random and deterministic jitter inside the delay-line are developed. In addition, several active and passive bandwidth extension schemes are analyzed and their simulations are presented. Independent design and characterization of a digitally-tunable delay-element with the best reported time-resolution of 1.25 ps is also provided. For the purpose of delay-stabilization of the delay-line, the design and measure-

ments of a wide-locking-range, 0.7-5 GHz, replica delay-line based delay-locked-loop (DLL) is also reported. One design version of this unique delay-line based data converter has also been demonstrated to function as a time-to-digital converter (TDC) with highest reported double hit resolution of 250 ps. Another version was designed and characterized as a 1:4 demultiplexer (Demux). Its comparison with other inductor-less 1:4 Demux designs shows the best achieved energy efficiency of 2.6 pJ/bit. In short, the presented delay-line based architecture has not only been demonstrated to work as a time-domain receive-side oversampling data converter but has also been proved to possess several other signal processing functionality.

Next, controlled capacitor charge/discharge based unique pulsewidth modulator (PWM) and de-modulator (PWDM) are presented. This PWM modulator works by controlling the discharge rate of a capacitor. The designed PWM modulator consists primarily of a 2-bit current-steering digital-to-analog converter (DAC) and a voltage-to-time converter (VTC). The VTC operates in two phases. First phase requires the capacitor to be charged to the supply rail, while the second phase discharges the capacitor using the control voltage generated by the DAC. The rate of the capacitor discharge defines the width of the output PWM pulse. The proposed PWM modulator is demonstrated to achieve data rates upto 10 Gb/s and a record energy efficiency of 0.9 pJ/bit. The complementary PWDM consists of a time-to-voltage converter (TVC) and a 2-bit analog-to-digital converter (ADC). TVC operates in the charge phase and the discharge phase. During the charge phase an input pulsewidth-modulated (PWM) signal charges a capacitor to a certain value. The larger the width of the PWM signal, the higher the voltage developed across the charged capacitor. This capacitor voltage, which is unique to each pulsewidth, is then digitized inside a 2-bit ADC. During the discharge phase, the capacitor is allowed to completely discharge to ground. The PWDM is demonstrated to achieve the best reported energy efficiency of 0.93 pJ/bit.

Finally, the tree-architecture based 4:1 multiplexer (Mux) and 1:4 Demux are designed and characterized. For the design of the latch, which is used primarily inside the key building blocks of the Mux and Demux, a power-speed optimized current-scaling methodology is provided. The results of an electromagnetic (EM) 3D field solver, which was used to simulate the high-frequency performance of the most critical data and clock paths inside the Mux and the Demux, are presented. In addition, a novel delay-line based highly scalable all-CMOS 16:1 Mux is presented and its simulations are provided. The design and analysis of this 25 Gb/s architecture shows that this delay-line Mux achieves an energy efficiency of only 160 fJ/bit, a near 10$\times$ improvement over the recently reported Muxes.

The time-domain converter circuits discussed in this thesis including the input-sampled delay-line data converter and its variants, PWM/PWDM and Mux/Demux circuit blocks present several novel circuit techniques and have been demonstrated to improve the state-of-the-art.

ZUSAMMENFASSUNG (ABSTRACT IN GERMAN)

***Note*:**
The German abstract does not contain word-to-word translation of the English abstract, but conveys the exact amount and breadth of information as the latter. The translation was composed with the help of several colleagues acknowledged in the previous section. For the acquisition of the first-hand knowledge of the abstract of this PhD thesis, I request you to please refer to the abstract in English.

Sami Ur Rehman

Die neuen 5G-Technologien und Internet-of-Things (IoT) Anwendungen führen zu Wachstumsraten des übertragenen Informationsvolumens von bis zu 8 % jährlich. Diese Entwicklung setzt neue Grenzen für die Infrastrukturen der existierenden Datenübertragungsnetze. Im Rahmen des Hardware-Designs werden sowohl für zellulare als auch für serielle Kurzstreckenverbindungen Transceiverschaltungen entwickelt, um eine höchstmögliche Energieeffizienz zu erreichen. Die Transceiver-Schaltungen bestehen im Wesentlichen aus analogen RF-Frontend Blöcken und Datenwandlern, die die digitalen Daten in analoge Signale umwandeln und umgekehrt. In den konventionellen Systemen konvertiert der Datenwandler auf der Senderseite der Verbindung die digitale Information in ein analoges Signal mit einer entsprechenden Amplitude um. Auf der Empfängerseite wird diese Amplitudeninformation zurück in digitale Daten umgewandelt. Allerdings weisen die Datenwandler in skalierten CMOS-Technologien Einschränkungen aufgrund des Aussteuerbereiches auf, da sie wegen begrenzter Durchbruchspannungen mit niedrigen Spannungen versorgt werden müssen. Somit wird die Rauschzahl des gesamten Netzwerkes beeinträchtigt. Eine Möglichkeit, dieses Problem zu beheben, ist die Umwandlung der Information auf der Empfängerseite in eine Zeit-Variable statt eine Amplituden-Variable. In dieser Arbeit werden mehrere energieeffiziente Zeitbereichsdatenwandler sowohl auf der Empfänger-, als auch auf der Senderseite in einem skalierten CMOS-Prozess entworfen.

Zunächst wird auf Empfängerseite ein eingangsseitig verzögerter Datenwandler mit hoher Überabtastung präsentiert, welcher auf einer Kette von Verzögerungsgliedern basiert. Diese hoch skalierbare, adaptive Multistandard-Datenwandlerarchitektur digitalisiert sowohl Schwellen und Schwellenübergänge als auch Abstände zwischen verschiedenen Übergängen für beliebige binäre Eingangssequenzen. Die Schaltung tastet verzögerte Kopien einer schwellenüberquerenden Bitsequenz innerhalb einer differentiellen Verzögerungsleitung ab. Das resultierende digitale Wort trägt Informationen zu den Schwellenübergängen sowie zu deren Abständen untereinander. Der verzögerungsleitungsbasierte Datenwandler kann jegliche Zeitbereichswellenform mit einer Energieeffizienz von 1,62 pJ/Bit überabtasten, was hinsichtlich des aktuellen Stands der Technik einen Rekord darstellt. Um Jitter zu minimieren, wurde das verwendete, Bessel-Filter basierte Verzögerungselement innerhalb der Verzögerungsleitung sorgfältig modelliert und entworfen. Außerdem wurden Methoden zur Erweiterung der Bandbreite analysiert und die entsprechenden Simulationsergebnisse vorgestellt. Darüber hinaus wurde ein digital steuerbares Verzögerungselement mit einer Zeitauflösung von 1,25 ps entworfen und charakterisiert, was ebenfalls einen Rekord darstellt. Um die Verzögerung der Leitung zu stabilisieren, wurde eine 0.7 - 5 GHz verzögerungsleitungsbasierter Delay-Locked-Loop (DLL) entwickelt und gemessen. Eine Version dieses Datenwandlers wurde als Zeit-Digital-Umsetzer (TDC) erfolgreich getestet, wobei eine Auflösung von 250 ps erzielt wurde. Dieses Resultat verbessert ebenfalls den Stand der Technik. Eine weitere Version wurde als 1:4 Demultiplexer (Demux) entworfen und charakterisiert. Im Vergleich zu anderen spulenlosen 1:4 Demultiplexern weist diese realisierte Schaltung die beste Energieeffizienz von 2,6 pJ/Bit auf. Zusammenfassend funktioniert die vorgestellte verzögerungsleitungsbasierte Architektur nicht nur als Überabtastungsdatenwandler, sondern realisiert zusätzlich auch mehrere weitere Signalverarbeitungsfunktionen.

Außerdem wurden ein Pulsweitenmodulator (PWM) und –demodulator (PWDM) entworfen. Diese Schaltungen beruhen auf dem Prinzip der gesteuerten Kondensatorauf- und -entladung. Der PWM basiert auf einer Steuerung der Kondensatorentladungsquote. Er besteht im Wesentlichen aus einem 2-Bit stromsteuernden Digital-Analog-Umsetzer (DAC) und einem Spannungs-Zeit-Wandler (VTC). Der VTC hat zwei Arbeitsphasen. In der ersten Phase wird der Kondensator bis zum Erreichen der Versorgungsspannung aufgeladen, während der Kondensator in der zweiten Phase anhand der vom DAC erzeugten Steuerspannung entladen wird. Die Pulsweite wird durch die Kondensatorentladungsquote bestimmt. Labormessungen zeigen, dass der entworfene PWM Datenraten von bis zu 10 Gb/s und eine Rekordenergieeffizienz von 0,9 pJ/Bit aufweist. Der PWDM setzt sich aus einem Zeit-Spannungs-Wandler (TVC) und einem 2-Bit Analog-Digital-Umsetzer (ADC) zusammen. Der TVC arbeitet in der Auflade- und Entladephase. Während der Aufladephase wird der Kondensator durch ein pulsweitenmoduliertes Eingangssignal bis zu einer bestimmten Spannung aufgeladen. Je breiter die Pulsweite des Eingangssignals ist, desto höher ist die Spannung über dem Kondens-

ator. Diese, einer Kondensatorspannung eindeutig zuordenbare Pulsweite, wird durch den ADC zu einem digitalen Signal umgewandelt. Während der Entladephase wird der Kondensator vollständig entladen. Der PWDM erzielt die bislang beste Energieeffizienz von 0,93 pJ/Bit.

Schließlich wurden ein 4:1 Multiplexer (Mux) und ein 1:4 Demultiplexer entworfen und charakterisiert. Für den Entwurf des Latches, welcher ein wesentliches Bauteil in Multiplexer und Demultiplexer ist, wurde eine Stromskalierungsmethode hinsichtlich Leistung und Geschwindigkeit optimiert. Für die kritischen Daten- und Taktsignalpfade wurden elektromagnetische (EM) Simulationen durchgeführt, um deren Hochfrequenzverhalten zu untersuchen. Zudem wurde ein neuartiger hoch skalierbarer 16:1 Multiplexer entworfen, welcher auf dem Prinzip der Verzögerungsleitungen basiert.

Die im Rahmen dieser Arbeit entworfenen Zeitbereich-Umsetzerschaltungen, wie z.B. der eingangsabtastende, verzögerungsleitungsbasierte Datenumsetzer und seine Varianten, die PWM/PWDM und Multiplexer/Demultiplexerschaltungen weisen mehrere neuartige Schaltungstechniken auf, die den Stand der Technik beträchtlich verbessern.

LIST OF ABBREVIATIONS

ACDE	Analog Controlled Delay-Element
ADC	Analog-to-digital Converter
ASK	Amplitude Shift Keying
BER	Bit Error Rate
BEOL	Back End Of Line
BJT	Bipolar Junction Transistor
BPSK	Binary Phase Shift Keying
BW	Bandwidth
BWER	Bandwidth Extension Ratio
CDR	Clock Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CML	Current Mode Logic
CS	Common Source
CSCP	Current Steering Charge Pump
DAC	Digital-to-Analog Converter
DC	Direct Current
DCDE	Digitally Controlled Delay-Element
DDJ	Data Dependent Jitter
DHR	Double Hit Resolution
DLL	Delay Locked Loop
DNL	Differential Non-linearity
DR	Dynamic Range
DSP	Digital Signal Processing
ENOB	Effective Number of Bits
EM	Electromagnetic
FF	Flipflop
FMC	FPGA Mezzaanine Card
FPGA	Field Programmable Gate Array

FSK	Frequency Shift Keying
FS	Full Scale
GD	Group Delay
HPM	High Performance Mode
ISI	Inter Symbol Interference
IoT	Internet of Things
LNA	Low Noise Amplifier
LPM	Low Power Mode
LSB	Least Significant Bit
LTI	Linear Time Invariant
MCML	MOS Current Mode Logic
MIM	Metal Insulator Metal
MSB	Most Significant Bit
MS-FF	Master-Slave Flipflop
MSM-FF	Master-Slave-Master Flipflop
NRZ	Non Return to Zero
OOK	On-off Keying
OSR	Oversampling Ratio
PDK	Process Development Kit
PISO	Parallel Input Serial Out
PRBS	Pseudo Random Binary Sequence
PLL	Phased Locked Loop
PVT	Process Voltage Temperature
PWDM	Pulsewidth Demodulator
PWM	Pulsewidth Modulation
RF	Radio Frequency
RMS	Root Mean Squared
RZ	Return to Zero
SA	Sense Amplifier
SAFF	Sense Amplifier Based Flipflop
SAR	Successive Approximation
SNR	Signal-to-Noise Ratio
SOI	Silicon on Insulator

SoC	System on Chip
SMA	Subminiature Versoin A
SR	Set Reset
TDC	Time-to-Digital Converter
TL	Transmission Line
ToF	Time of Flight
TVC	Time-to-Voltage Converter
UI	Unit Interval
ULPM	Ultra Low Power Mode
VTC	Voltage-to-Time Converter

LIST OF SYMBOLS

A_k	Binary amplitude of the time-domain symbol
A	Amperes i.e. unit of current
A/m	Amperes per meter i.e. unit of current density
b/s	Bits per second i.e. unit of data rate
C_{CD}	Capacitance used in capacitive degeneration circuit
C_{db}	Drain to bulk capacitance
C_{fb}	Feedback Capacitor
C_{gd}	Gate to drain capacitance of MOS transistor
C_{gs}	Gate to source capacitance of MOS transistor
C_L	Parasitic load capacitance
Clk	Sampling clock used inside delay-line Mux
C_{PWM}	Charge/discharge capacitance in PWM modulator
C_{PWDM}	Capacitance used in PWM demodulator
C_{SEL}	Parasitic load used inside the selector block of PWM modulator
C_{ox}	MOS Oxide capacitance
D_{IN}	Data input to demultiplexer
e_t	Time-domain data converter error
F	Farad i.e. unit of capacitance
f	Signal frequency
f_{CLK}	Off-chip applied clock signal
g_m	MOS transconductance
H	Henry i.e. unit of inductance
Hz	Hertz i.e. unit of frequency
I_B	Bias current through CML inverter
I_{D1}	Capacitor charging current inside the PWM modulator
I_{D0}	Capacitor discharging current inside the PWM modulator
I_P	PMOS current
I_N	NMOS current

I_{REF}	Reference current
I_{SS}	DC bias current
i_n^2	Current noise power
J/bit	Joules per bit i.e. unit of energy figure
K	Process dependent constant in flicker noise model
L	Length of the transistor
m	Meters i.e. unit of length
m	Ratio of the location of dominant zero to dominant pole
N_{inv}	Number of inverters inside a delay-element
n	Number of delay-elements in the replica delay-line
P_{LOAD}	PMOS current load
Q_{CHA}	Charge on a capacitor during during charging phase
Q_{DIS}	Charge on a capacitor during during discharging phase
R	Resistive load inside the current-mode-logic circuits
R_{CD}	Resistance used in capacitive degeneration
R_{ON}	On-resistance of the MOS transistor
R_{SEL}	Resistive load used inside the selector block of PWM modulator
REF_{SIG}	Externally-applied reference signal
$S_{in}(f)$	Input thermal noise power
$S_{out}(f)$	Outupt jitter power
$S_{X,Y}$	S-parameters, where X and Y represent port numbers
s	Second i.e. unit of time
s	A generic symbol in the time-domain input symbol sequence
s_{IN}	Input symbol
s_{REC}	Reconstructed symbol
T_{CLK}	Reference clock period
T_{HIGH}	Logic high width of a reference signal
T_{IN}	Minimum distance between two transitions inside the symbol sequence
T_{LOW}	Logic low width of a reference signal
T_{PWM}	PWM input signal
T_{SAMP}	Sampling resolution
t_a	Capacitor discharge time inside the PWM modulator
t_b	Capacitor charge time inside the PWM modulator

t_r	Rise time
υ_n^2	Voltage noise power
V_B	Externally applied bias voltage for delay-element
$V_{B,opt}$	Optimal value of the bias voltage
V_{CAP}	Voltage across the capacitor
$V_{CAP,PWDM}$	Voltage developed across PWDM modulator capacitor
V_{CNTRL}	Control voltage for the CMOS delay-line
V_{DAC}	DAC voltage
V_{eff}	Effective voltage
V	Volts i.e. unit of voltage
V_{TH}	Threshold voltage
V/s	Volts per second i.e. unit of slew rate
W	Watt i.e. unit of power
W	Width of the transistor
X	Number of delay-elements inside the delay-line
Z_{in}	Input impedance
Z_O	Characteristic Impedance
Δ	Amplitude resolution of an ADC
ΔT	Minimum distance between two transitions inside the symbol sequence
ΔV	Output signal swing
λ	Channel length modulation factor
μ	Ratio of input clock period to the input symbol period
υ	Sum of similar consecutive bits in the digital bit stream
τ	Delay of a single delay-element
τ_a	Delay of an active delay-element
τ_{CAL}	Calculated value of delay of the delay-element
τ_{dmx}	Delay of a delay-element inside delay-line based Demux
τ_{MEA}	Measured value of delay of the delay-element
τ_p	Delay of passive delay-element
τ_{opt}	Optimal value of the delay
ψ	Delay of the data converter delay-line
ψ_{dmx}	Delay of the Demux delay-line
Ω	Ohms i.e. unit of resistance

NOTE ON THE USE OF OWN IEEE MATERIAL

The contents from chapter 2 to chapter 6 of this dissertation are, up to 50% - 60%, based on the already published IEEE papers in which I have been the first author. These IEEE papers were published during the time of my doctoral research at TU Dresden. I have referenced all the published papers in the text properly in accordance with the IEEE copyright policies, and have also included a list of these IEEE papers at the end of my dissertation. This list is titled as the "List of Own Publications". In addition, a footnote at the beginning of each chapter clearly mentions which sections borrow material from the self-authored papers. To explicitly distinguish them from other citations in the text, tables and figures referenced in the thesis chapters, the citations for the own self-authored papers are superscripted with a special symbol i.e. ♣. For instance, a self-authored paper [X] is cited in the thesis as [X]♣.

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CHAPTER 1

DATA CONVERSION IN TIME-DOMAIN

The ever-increasing energy requirements of any broadband and high-speed digital communication architecture presents an area of concern for system architects, digital signal processing (DSP) engineers and hardware designers. With the rapid rise of mobile based web-browsing and the use of cloud computing for storage and processing of data in globally distributed data centers, the energy consumed by data networks and servers has increased tremendously. The worldwide annual growth rate of information and communication technology, for example, is around 7% [1] and, specifically, for internet traffic is around 22% [2]. Such an alarming growth rate is driving the data rates up to 100 Gb/s while putting stringent power and performance constraints on the entire communications infrastructure. In the domain of hardware design, several spectral-efficient wideband chip-to-chip and board-to-board wireline [3], [4] and wireless [5], [6] serial communications links are investigated to address this challenge of energy-performance tradeoff for server computing application and processor inter-core communication. However, for such advanced architectures, ultra-wideband operation and the corresponding ultra-high speed sampling poses challenging requirements on the circuit-level design of data converters used in such links. This requirement has motivated research on many remarkable high-speed multi-bit data converter architectures [7], however, the excessive power and area consumption of these converters and their degraded signal-to-noise ratio (SNR) at higher speeds renders them unsuitable to be used in multichannel beamforming application setups such as chip-to-multichip communications on two adjacent boards. This restriction has driven the need to investigate alternate data converter architectures.

1.1 Communications System Overview

Fig. 1.1 shows a generic overview of a wireless and wireline communication link. Data converters in both the links sit in between the digital processing backend and the RF front end. Wireless links typically employ multibit digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) inside the transmitter and receiver respectively. A wireline optical or electrical link, on the other hand, time-interleaves or pulse-modulates the data on the transmitting link and utilizes clock-data recovery (CDR) based demodulation to recover or reconstruct the transmitted symbols in time.

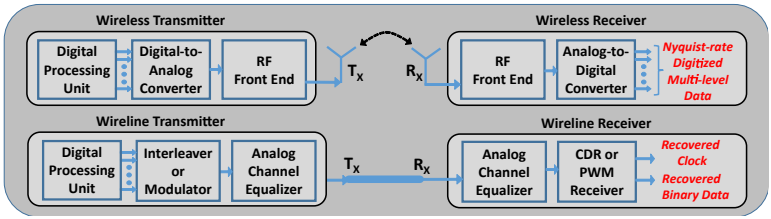

Figure 1.1: Conventional wireline and wireless transceiver architectures.

1.2 Data Conversion in Communications

Data converters are circuits which convert the information-bearing data contained in one measurable physical quantity into another. Smart data converters convert analog data into digital format or the digital data into analog format. For instance, a bipolar junction transistor (BJT) temperature sensor core translates the temperature into the difference of base-emitter voltages and can, by definition, be referred to as temperature-to-voltage converter. Using an ADC to converter the sensed voltage difference into a digital format would result in a smart temperature sensor. Typically, however, the term data converter refers to smart data converter, which either generates or acquires the digital data for processing.

Within communications paradigm the data converters either convert digital data into amplitude or time domain, for instance, DACs or pulsewidth modulators respectively, or convert the amplitude or time domain data into digital format, such as ADCs or CDR based PWM demodulators respectively. Therefore, in communications system the analog information is available either in amplitude-domain, like the different amplitude levels of a pulse [8], or time-domain, such as the different widths of a binary pulse or its time-distributed zero-crossings [9]♣.

1.3 Data Conversion: From Amplitude to Time Domain

To achieve enhanced data rates and higher channel spectral efficiency, wireless serial links typically employ multi-amplitude modulation schemes, and hence, require multi-bit/amplitude-domain data converters i.e. ADCs and DACs. Fig. 1.2 shows, as an example, the assignment of analog values to the input digital codes inside the DAC and the resulting baseband signal at its output. The baseband signal is modulated to a carrier frequency inside the RF front end and transmitted over a wireless link. The receiver front end demodulates the carrier signal, and if sufficiently linear, regenerates the exact replica of the baseband signal at the input of the ADC.

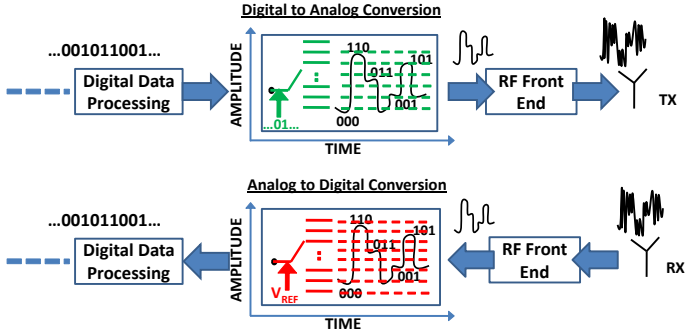

Figure 1.2: A traditional wireless link employing an ADC and a DAC in receiver and transmitter side respectively. DAC translates digital input into different amplitude levels while the ADC translates back the amplitude levels to digital format (code conversion may be necessary to extract the exact transmitted bits).

The ADC performs the exact opposite operation as the DAC. It samples the received baseband signal at Nyquist or higher rate, and assigns each sample a unique digital signature or code. Each binary code has a length of N bits, resulting in 2^N available codes to be assigned to the analog signal. This ADC output is the digital binary coded representation of the analog signal. The left most bit of the digital code is referred to as the most significant bit (MSB), while the rightmost bit is called the least significant bit (LSB), which is typically called the resolution of the ADC. The step size on the vertical axis of the ADC characteristics plot, Δ, is equal to the analog value of the LSB and the entire axis or the conversion range is referred to as the full scale (FS) range or the analog dynamic range (DR) of the converter. The FS range is defined as the range of analog input values which can be reliably digitized inside the ADC without causing any saturation issues and depends not only on the power supply voltage but also on the data converter circuit topology. Typically, data converters are designed for maximum achievable FS range, which is usually the available supply voltage. The converter's

resolution as a function of it's FS range can be written as

$$\Delta = \frac{FS}{2^N} = \frac{DR}{2^N} \tag{1.1}$$

1.3.1 Technology Scaling and Amplitude-Domain Data Converters

CMOS technology scaling is always aimed at maximising the performance of the digital systems, rendering the design of the analog circuits challenging, owing to the reduced available voltage headroom. This is because the threshold voltage of the devices scales down rather slowly in comparison to the aggressive voltage scaling, which essentially reduces the difference between available supply voltage and minimum voltage required to keep the stacked transistors in saturation with each scaled node. While minimum feature size of CMOS transistors enables miniaturization of microprocessors and the digital processing chips, and offers high performance, this technology scaling presents serious constraints in the design of mixed-signal circuits such as data converters due to reduced voltage headroom. In the receiver side, for instance, the ultra-high speed sampling of multi-amplitude modulated input, poses challenging requirements on the circuit-level design of the multi-bit ADCs [7]. This is because the decreasing minimum feature size of modern CMOS processes forces such traditional multi-bit voltage-mode ADCs - and of course DACs - to operate from lower supply voltages to meet device-breakdown requirements. While this is beneficial for the power dissipation, it affects the amplitude-domain quantization, effectively increasing the thermal noise floor and reducing the dynamic range or the SNR, which eventually worsens the overall noise figure of the transceiver architecture [10]. This can be intuitevely understood by examining (1.1). An N-bit ADC designed in 0.5-μm CMOS node can have a FS range up to 3 V compared to the one designed in, say, 45-nm node, in which case the maximum achievable FS range would be around 0.9 V. Therefore, for the same resolution ADCs, technology scaling from 0.5-μm node down to 45-nm node nearly reduces the FS range and the corresponding analog resoluton, Δ, by a factor of three. This reduced Δ renders the ADC to become more suseptable to the quantization noise due to, for instance, the aperture jitter of the sampling clock. Resultantly, the accuracy of the amplitude-domain data converters, which depends on minimum detectable voltage or Δ, scales poorly with technology. In addtion, the data converters circuit components designed at lower power supply in submicron technologies are more prone to process voltage temperature (PVT) variations and can contribute significant thermal noise to the the signal. This resultantly increases the noise floor of the ADC, which effectively reduces the SNR or the effective number of bits (ENOB) of the ADC designed in scaled CMOS nodes. The reduced SNR of the ADC worsens the overall noise figure of the receiver. Besides the degraded SNR of the data converters in scaled CMOS nodes, excessively high power consumption of such ADCs, such as [7], [11], precludes their use in multichannel beamforming serial link

environments, which are increasingly being investigated to satisfy the growing performance requirements inside the backplane server computing setups and processor inter-core serial links.

1.3.2 Amplitude-Domain Data Converters: Tradeoff between Dynamic Range and Bandwidth

An interesting insight into the functionality of a generic data conversion architecture is the interpretation of the tradeoff between its dynamic-range (DR), defined by the quantized amplitude levels on the vertical scale, and its bandwidth, defined by the discrete sampling time instants on the horizontal scale, as shown in Fig. 1.3. In the context of this DR-bandwidth or amplitude-time tradeoff, data converters can be classified into three key categories. The following qualitative analysis is presented for the amplitude-domain receiver data converters or multi-bit ADCs but could very well be interpreted for transmitter data converters or multi-bit DACs.

The first category consists of conventional clock-synchronized ADCs in which the analog input is represented by evenly distributed amplitude-time ordered pairs, as can be seen in Fig. 1.3(a). Such ADCs can be sub-categorized in two groups: a) voltage-mode ADCs and b) voltage-time hybrid ADCs. In case of voltage-mode ADCs, the time-varying analog input is first sampled and the resulting voltage is then quantized; while in the second class the sampled voltage variable is converted into a time variable, which is then digitized in time-mode circuits. Concerning voltage-mode ADCs, different architectures are preferred for different specifications e.g. noise shaping ADCs are used in high-resolution low-frequency applications [12]. For medium-resolution and medium sampling speed, SAR ADCs are preferred [13], [14]. High-speed low-resolution applications typically employ flash ADCs [15], [16]. High-speed and medium-to-high resolution applications usually require pipelining [17]. Finally, for ultra-high-speed and medium-resolution applications, SAR or flash ADCs can be interleaved [18], [7]. For voltage-time hybrid ADCs, the sampled voltage is first converted into a time variable, e.g. the width of a pulse, and later the time variable is digitized in what is known as Time to Digital Converter (TDC). A dedicated Voltage to Time Converter (VTC) circuit is used to convert the voltage-variable into a time-variable [19], [20].

For balanced distribution of amplitude-time pairs, this category of ADCs employ sample-and-hold (S/H) circuits at their front-ends. For ultra-high frequency operation, this makes the performance of these ADCs susceptible to the artifacts introduced by the sampling process, such as aliasing, noise folding, and aperture jitter in the sampling clock. While time-interleaved ADCs enable sampling rates up to tens of GS/s, their performance is limited by several factors including clock jitter and skew, geometric mismatch among channels, gain

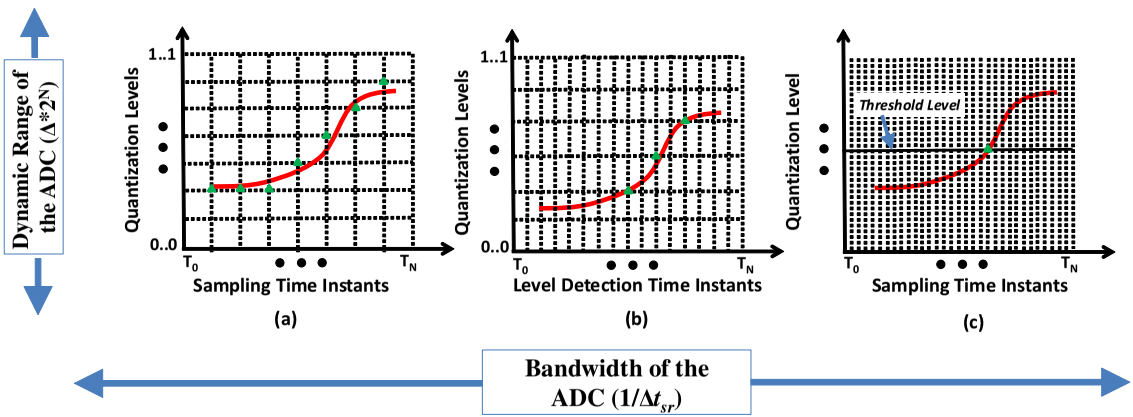

Figure 1.3: Three different categories of receiver data converters showing a tradeoff between amplitude dependent dynamic-range and sampling-resolution dependent bandwidth. Here Δt_{sr} represents the sampling resolution and equals the time-distance between two consecutive vertical lines in each plot.

and offset mismatch among sub-ADCs, and capacitive loading to the sampling stage by the interleaving array [21]. Such designs, therefore, resort to design-intensive error correction (calibration, redundancy and randomization techniques) and linearity improvement (gain and offset correction) circuit techniques, which cause power, area and design overhead [21]. In addition, as discussed before, this category of ADCs suffers from reduced SNR in scaled CMOS nodes.

The second category includes architectures in which the DR of the ADC is traded off, to some extent, in favor of its BW as shown in Fig. 1.3(b). For example, to achieve a certain resolution, Nyquist sampling requires lowest ADC bandwith but more quantization levels (Fig 1.3(a)). Oversampling and utilizing a lower number of quantization levels, as shown in Fig 1.3(b), can achieve the same resolution [22]. Reported ADCs, which exchange amplitude for time to some extent, do not have evenly distributed amplitude-time ordered pairs and are typically referred to as asynchronous/clock-free ADCs, level-crossing ADCs or event-driven ADCs [23]. Such ADCs only record samples when the input signal crosses a quantization level. Since, such data-converters rely on event-driven sampling dictated by the message signal itself, and use level-crossing comparators to detect the crossing event instead of employing an external sampling clock, their use is limited to low power, high-resolution, and low-frequency design regime, which renders them unsuitable for ultra-wideband operation. In addition, technology-scaling-caused SNR reduction still remains a problem.

Following the ADC categories discussed above and their key limitations, it can be comfortably argued that the continuous scaling of the CMOS process has resulted in increased time-resolution and reduced voltage or amplitude-resolution. To address the scaling-induced performance degradation of the data converters, it is convenient, on the transmitting side, to translate the data into time difference between the occurrences of digital events/data instead of nodal voltages or branch currents of electric circuits. Consequently, on the receiving side, amplitude scale can be completely turned over to time scale, and hence, quantization can be performed in time domain instead of amplitude domain. This scheme presents a viable option to circumvent some of the above problems concerning the first two categories of the ADCs. Therefore, a third category of data converters is defined which presents the limit case of amplitude-to-time conversion as can be seen in Fig. 1.3(c). Data conversion circuits under this category deal only with binary antipodal signals and perform quantization in time domain as the converter DR is reduced to just one predefined quantization level. It is argued that exchanging the quantization scale from amplitude to time-domain can help in scaling-caused dynamic range reduction issue in the data converters of the first two categories.

1.3.3 Existing Time-Domain Data Converters and their Limitations

Serial links which operate under the limit case of amplitude-to-time conversion deal only with binary symbols and perform quantization in time domain as the amplitude dynamic range of the input is reduced to just one predefined quantization level (third category data converters depicted in Fig. 1.3(c). The transmitting side of such a link either serializes the input parallel streams e.g. multiplexing non-return-to-zero/return-to-zero (NRZ/RZ) input symbols [3] or modulates the width of a pulse [4]. The receiving side of the link is designed to distinguish the relative position of the transmitted symbols in time. Examples of such receivers, typically employed in a wireline link, include a CDR circuit and a demultiplexer-based receiver, and PWM demodulators. CDR and PWM demodulators deal with symbols, which carry information in their binary amplitude levels e.g. RZ/NRZ signaling symbols, and pulse-widths e.g. PWM symbols. Such time-mode receivers first recover the clock embedded in the input symbols and then use this recovered clock to sample the received symbols, under the assumption that each symbol spans equal amount of time. However, channel losses, limited link bandwidth, and analog circuit impairments result in inter-symbol-interference (ISI) or jitter, corrupting the transmitted value of symbols time-length or the distance between transitions. In addition, such time-mode receivers are typically based on phased-locked-loop (PLL) design whose high-speed performance is limited by design challenges including input sensitivity, jitter tolerance, signal distribution, analog circuit non-idealities, power dissipation etc [24]. These limitations not only restrict the input data-rate range but also make the signal reconstruction a challenging task at speeds in the order of tens of Gb/s. For reliable clock and data recovery, such receivers, therefore, resort to analog-intensive equalization schemes [25] and require pre-emphasis/equalization on the transmitting side as well. A promising technique of precisely recovering the time-mode binary symbols, while minimizing the equalization overhead, is to oversample the received input symbol sequence [26]. However, implementing oversampling in the existing time-domain data converters comes at the cost of design overhead and incurs a heavy power penalty [26].

1.4 Thesis Motivation and Organization

To this point it has been established that performing quantization in time-domain instead of amplitude-domain can circumvent the problem of reduced dynamic range in multi-bit data converters designed in submicron CMOS. This amplitude-to-time conversion, however, requires the information or data to be translated in a time variable instead of a voltage variable. The data converters which deal with such time-domain data were also discussed and the limitations in their architecture were presented. These limitations prevent such convert-

ers, on the receiving end, to recover the time-domain data with high precision without the use of power-area hungry analog-intensive equalization circuitry. In addition, implementing power-speed tunability in existing time-domain converters comes at the cost of additional design and power-area overhead, precluding their use in hotly-researched and promising future-generation energy adaptive serial links architecture, such as [27].

The work presented in this thesis has primarily been motivated by the above-mentioned limitations, inspiring us to investigate new power-area efficient and power-speed adaptable time-domain data converter architectures suitable for transmitting and receiving the time-domain data with sufficiently high precision. The following chapters in this thesis consist of circuit techniques and architectural novelties aimed at addressing the limitations of the existing time-domain data converters.

Chapter 2 discusses a novel delay-line based high oversampling time-domain data converter. The chapter starts with an overview of the significance of oversampling on time-mode data, details the architecture and circuit level design of the data converter, presents its characterization results and finally compares it with the existing time-domain converter circuits. Chapter 3 discusses in detail the some of the key applications of the data converter discussed in chapter 2. It also provides details on the wireless serial link demonstrator setup in which the data converter was used as an oversampling quantizer on the receiver side. Chapter 4 discusses improvements made on the basic delay-line based receiver data converter. These include automatic delay control of the delay-line using a delay-locked-loop (DLL), implementing inductive peaking inside the delay-elements of the delay line and making them power-speed adaptable. Chapter 5 discusses pulsewidth modulation/demodulation based data converters. The chapter details a novel capacitor charging/discharging based PWM modulator

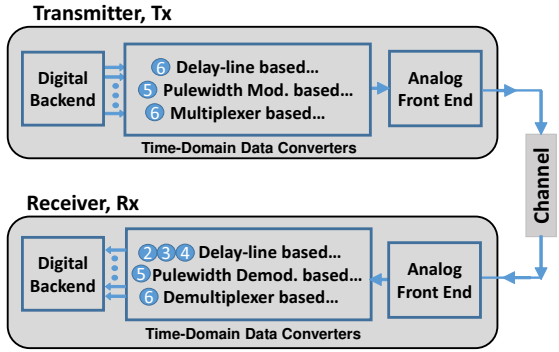

Figure 1.4: Data converters on the transmitter and receiver side designed as a part of this thesis work. The numbered circle besides each data converter indicates the chapter in which it is discussed.

and demodulator which has been characterized to achieve best energy figure in comparison to the existing PWM architectures. Chatper 6 explores broadband tree architecture and shift register architecture based multiplexer and demultiplexer based data converter designs. It also presents a delay-line based transmitter data converter which works on the principle exactly opposite to that of the delay-line based receive data converter discussed in chapter 2. This converter architecture can achieve data rates upto 25 Gb/s, with a power efficiency of only 160 fJ/bit. Finally, the conclusion and future outlook of time-domain data converters is brought up in Chapter 7.

Fig. 1.4 shows different types of the time-domain data converters designed in this work for transmit and receive channel. Delay-line based data converters are presented in chapters 2-4 and 6, while the PWM modulators/demodulators and multiplexers/demultiplexers are discussed in chapter 5 and 6 respectively.

1.5 Few Words on the GLOBALFOUNDRIES 45-nm SOI CMOS Process Node

The circuits and systems presented in this work were designed and characterized in GLOBALFOUNDRIES (GF) 45-nm silicon-on-insulator (SOI) technology and its upgraded RF flavor 45RFSOI. The technology has been extensively used in the design and characterization of several broadband RF and mixed signal circuits including low-noise amplifiers (LNAs), high-speed multiplexers, wireline transceivers, and power amplifiers to name a few [28], [29]. The process offers partially depleted floating body NMOS and PMOS devices while the channel length is fixed at 40-nm. Two gate oxide thicknesses are available: a thin oxide gate with a nominal supply voltage of 0.9 V and a thick oxide gate with a nominal supply voltage of 1.5 V.

Besides the commonly included pcells, the provided process development kit (PDK) includes high quality metal-insulator-metal (MIM) capacitors, high-Q inductors and RF modelled transmission lines. Up to four back-end-of-line (BEOL) metal stacks are available with minimum seven metal layers for one stack (7LM-3Mx-1Cx-1Ux-1Ox-LD) and upto eleven metals for another (11LM-3Mx-2Cx-3Bx-2Ux-LB). The process also offers different gate poly pitches allowing the relaxed poly pitch transistors to benefit from reduced parasitics due to larger separation between source/drain contacts and the gate poly. According to the measurement data provided by the original developers of the process, for 30 μm wide NMOS and PMOS - 30 fingers with each 1 μm wide for both transistors - peak f_t of 485 GHz and 345 GHz can be achieved respectively in this process. This demonstrates the intrinsic broadband nature of the active devices available in this process.

This 45-nm CMOS process, originally developed by IBM, includes several IBM-designed

digital-oriented pcells and also GF-introduced analog/RF-oriented pcells. This makes this process an ideal candidate for the design and development of System-on-Chip (SoC) architectures.

1.6 Chapter Summary

This chapter started with the discussion of the ever increasing internet and mobile traffic and the power and performance constraints these data requirements are placing on the existing hardware infrastructure. In order to address this exponential growth in demand of data traffic in both short-haul and long-distance wireless and wireline links, the importance of broadband circuit design was discussed. Next, the amplitude-domain and time-domain data converters were presented and it was argued that due to technology scaling the dynamic range of amplitude-domain data converters is decreasing while the noise floor is consistently increasing. After examining the dynamic range and bandwidth trade-offs between of the amplitude-domain converters, it was proposed that performing quantization in time-domain can potentially solve the technology-scaling-caused SNR reduction in amplitude-domain data converters. Next, some existing time-domain data converters and their limitations were discussed and a motivation to work on energy-efficient high-precision time-domain circuits was presented. Finally, some qualities of 45-nm SOI CMOS node were discussed, which is primarily used to fabricate the circuits designed and characterized in this dissertation.

In the following chapters several new time-domain transmit- and receive-side designed and characterized data converter circuits are presented and their improved specifications over the state-of-the-art are discussed.