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Sönke Vehring

Microwave Circuits in Bulk and Fully-Depleted Silicon-on-Insulator CMOS Technologies

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Abstract

This work presents microwave circuits in 65 nm bulk, and 22 nm fully depleted silicon-on-insulator (FDSOI) complementary metal-oxide-semiconductor (CMOS) technologies. In the first part of the thesis, the work explains the microwave properties of the two state-of-the-art CMOS technologies and gives reasons why CMOS is nowadays attractive for microwave circuit design. The second half shows front-end circuits designed for two research projects.

The first project consists of a quadrature-phase receiver and a high-efficiency transmitter in 65 nm bulk CMOS for a 24 GHz localization system based on the secondary radar principle. The receiver circuitry includes a low-noise amplifier (LNA), poly-phase network, and passive down-converter with post-amplifier. In the LNA, a new method is used, which, despite process tolerances and model uncertainties, maximizes the gain in a target frequency band. The receiver employs a poly-phase network realized by a small directional coupler based on lumped elements. New is here that the coupler omits the termination of the isolated port reducing noise in the receiver. Furthermore, the system uses frequency doubling of the local oscillator (LO) to enable the operation of a digital phase-locked loop (PLL) with low phase noise. Therefore, this work introduces the first truly balanced push-push (PP) frequency doubler, which allows mbesides for high output power, high efficiency, and high suppression of the fundamental wave at the same time.

The second project aims at a broadband receiver, which covers the complete W-band from 75 to 110 GHz for future 100 Gb/s wireless communication. The receiver utilizes a frequency quadrupler to multiply an 18.5 GHz LO signal for downconversion of the W-band RF frequencies to 1 to 36 GHz intermediate frequencies (IF). The quadrupler cascades two truly balanced PP doublers designed in 22 nm FDSOI CMOS. Furthermore, the PP doublers use a more efficient floorplan, which results in lower chip area consumption.

Zusammenfassung

In dieser Arbeit werden Mikrowellenschaltungen in 65 nm Bulk Complementary Metal-Oxide-Semiconductor (CMOS) und 22 nm Fully-Depleted Silicon-on-Insulator (FDSOI) Technologien vorgestellt. Zunächst werden die Mikrowelleneigenschaften der beiden modernen CMOS Technologien erläutert und Gründe angegeben, warum CMOS heutzutage für das Design von Mikrowellenschaltungen attraktiv ist. Zweitens zeigt die Arbeit Front-End Schaltungen, die für zwei Forschungsprojekte entwickelt wurden.

Das erste Projekt besteht aus einem Quadraturphasenempfänger und einem hocheffizienten Sender in 65 nm Bulk CMOS für ein 24 GHz Lokalisierungssystem, das auf dem Sekundärradarprinzip basiert. Die Empfängerschaltung umfasst einen rauscharmen Verstärker (LNA), ein Mehrphasennetz und einen passiven Abwärtswandler mit Nachverstärker. In der LNA wird eine neue Methode verwendet, die trotz Prozesstoleranzen und Modellunsicherheiten die Verstärkung für eine Zielfrequenz mit wenigen Entwurfsläufen maximiert. Der Empfänger verwendet ein Poly-phasen-Netzwerk, das aus einem kleinen Koppler besteht, der auf konzentrierten Elementen basiert. Neu ist hier, dass der Koppler die Terminierung am isolierten Tor weglässt, um das Rauschen im Empfänger zu reduzieren. Darüber hinaus verwendet das System die Frequenzverdopplung des lokalen Oszillators (LO), um den Betrieb eines digitalen Phasenregelkreises (PLL) mit geringem Phasenrauschen zu ermöglichen. In dieser Arbeit wird daher der erste echt balancierte Push-Push (PP) Frequenzverdoppler vorgestellt, der eine hohe Ausgangsleistung, einen hohen Wirkungsgrad und eine hohe Unterdrückung der Grundwelle ermöglicht.

Das zweite Projekt zielt auf einen Breitbandempfänger ab, der das gesamte W-Band von 75 bis 100 GHz für die zukünftige drahtlose Kommunikation mit 100 Gb/s abdeckt. Der Empfänger verwendet einen Frequenzquadrupler, um ein 18,5 GHz LO-Signal zu multiplizieren für die Abwärtsmischung der W-Band RF Frequenzen auf 1 bis 36 GHz Zwischenfrequenzen. Der Quadrupler kaskadiert zwei echt balancierte PP-Verdoppler, die in 22 nm FDSOI CMOS entworfen sind. Darüber hinaus verwenden die PP-Verdoppler einen effizienteren Grundriss, was zu einem geringeren Verbrauch an Chipfläche führt.

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Finally, I want to express my deepest appreciation to my wife, Katharina, for her endless support to my professional development. Without you it would never have been possible to finish this work.

Berlin and Dresden, October 2022 *Sönke Felix Vehring*

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Acronyms

FMCW	Frequency-modulated continuous wave
BW	Bandwidth
FSPL	Free-space path loss
LOS	Line-of-sight
EM	Electro-magnetic
IC	Integrated circuit
PCB	Printed-circuit board
LNB	Low-noise block
ADAS	Advanced-driver assistance systems
ISM	Industrial, scientific, and medical
ITU	International telecommunications union
5G	Fifth generation of wireless communications
LO	Local oscillator
EIRP	Equivalent isotropic radiated power
CMOS	Complementary metal-oxide-semiconductor
PLL	Phased-locked loop
VCO	Voltage-controlled oscillator
ADPLL	All-digital phased-locked loop
DCO	Digitally-controlled oscillator
IQ	In-phase and quadrature-phase
SISO	Single-input single-output
MIMO	Multiple-input multiple-output
QAM	Quadrature-amplitude modulation
SiP	System in package
CPA	Circular-polarized antenna
SCDCR	Single-chip dual-channel receiver
ADC	Analog-to-digital converter
FDSOI	Fully depleted silicon-on-insulator
BEoL	Back-end of line
SNR	Signal-to-noise ratio
BER	Bit-error-rate
PSK	Phase-shift keying
AMS	Analog and mixed-signal circuits

LNA	Low-noise amplifier
PGA	Programmable-gain amplifier
ITRS	International technology roadmap for semiconductors
FET	Field-effect transistor
RDL	Redistribution layer
PGS	Patterned ground shield
BALUN	Balanced-unbalanced converters
MIM	Metal-insulator-metal
MOM	Metal-oxide-metal
GC	Gilbert cell
PA	Power amplifier
PP	Push-push
PPD	Push-push doubler
PAE	Power-added efficiency
ESD	Electro-static discharge
TC	Trimming cell
MN	Matching network

Mathematical Symbols

σ	Range resolution increment
c	Speed of light
BW	Bandwidth
f_b	Data-rate
L_{FSPL}	Free-space path loss
d	Distance
L	Leeson's phase noise
k	Boltzmann constant
T	Temperature
P	Power
f_c	Carrier frequency
Q	Quality factor
f_m	Offset-frequency from carrier
m_{LOS}	Mismatch line-of-sight
f_{max}	Maximum frequency
S	Signal power
G	Gain
N	Noise
SNR	Signal-to-noise ratio
Z	Impedance
NF	Noise figure
J	Current density
K_n	Transistor constant nFET
W_f	Transistor finger width
N_f	Transistor number of finger
L_g	Transistor gate length
gm	Transconductance
SRF	Self-resonance frequency

Contents

Chapter 1
Introduction

1.1 Why are microwaves attractive?

In general, more bandwidth (BW) is available at higher carrier frequencies in the frequency spectrum [1].

In case of a frequency-modulated continuous wave (FMCW) radar, using triangle modulation the range resolution increment σ is given by

$$\sigma = \frac{c}{2BW} \tag{1}$$

where c is the speed of light and BW is the modulation bandwidth. With larger bandwidth BW, the range resolution increment of the radar is decreasing, which in turn improves the accuracy of the distance measurement.

In case of a communication system the theorem of Shannon-Hartley determines the data-rate f_b and reads

$$f_b = BW \log_2 \left(1 + \frac{S}{N}\right). \tag{2}$$

The data-rate increases proportional with the absolute bandwidth. Therefore, the trend towards higher operating frequencies in radar and communication is unbroken.

However, the limitation in choosing an ever higher operating frequency is the free-space path loss (FSPL) L_{FSPL}. FSPL is the attenuation along a line-of-sight (LOS) with distance d from transmitter to receiver and perfect alignment

$$L_{FSPL} = \left(4\pi d \frac{f}{c}\right)^2. \tag{3}$$

With a high carrier frequency, the FSPL can be so high that the specification on the transmitter and receiver in a foreseen application requires for expensive technology, large chip area, and high design effort.

The term microwave is a combined word of the micro (greek, mikros: small, short) and electromagnetic waves. Conventionally, the free-space wavelength for microwaves is 1 mm to 10 cm, which corresponds to frequencies between 3 and 300 GHz [2]. Others include wavelengths up to 5 dm also to microwaves, which extend the frequency range down to 600 MHz. Frequencies, with wavelengths from 1 to 10 mm, are known as mm-waves and are thus part of microwaves.

Microwave circuit design is challenging since the dimensions of the electronic devices are in the order of a tenth of a wavelength or more. Therefore, voltages and currents are not constant over the devices. Along the physical dimensions of the electronic devices, linear elements such as capacitors, inductors, and resistances are distributed. That is why, these electronic devices are referred to as distributed elements. Distributed elements must be precisely modeled for accurate impedance-transformations to achieve the desired power or noise matching. Electro-magnetic (EM) simulation or measurement of known test-structures support the precise modeling of distributed elements. An example of a distributed element is the transmission line. Besides distributed elements, there are electronic devices that are much smaller than the wavelength, exhibiting a frequency-dependent behavior due to parasitic linear elements. These devices are referred to as quasi-lumped elements due to the parasitic effects. As with the distributed elements, a great deal of effort has to be made to correctly determine the quasi-lumped elements over the frequency of interest for a successful power or noise matching. Since matching by reactive and susceptive elements is frequency-dependent, the design process is about tuning the performance in a specific frequency band. Most importantly, all electronic devices have to be realized with high precision, such that they follow the modeled behavior. Fortunatelly. the challenge of microwave circuit design is significantly relaxed by using technologies with small dimensions and tight tolerances. This reduces the amount of distributed elements and lowers parasitic effects with quasi-lumped elements. Furthermore, the low tolerance enables reproducible manufacturing with high yield.

With the emergence of integrated circuit (IC) technologies, the physical dimensions, as well as manufacturing tolerances, have been dramatically decreased compared to printed-circuit board (PCB) technologies. Therefore, rather expensive IC technologies are widely used for microwave circuits in order to minimize the challenge of microwave circuit design and enable reliable performance. IC technologies involve high single-time costs for the production of the mask sets. Low market-demand applications, which can afford the high technology costs, are mostly of military purposes. Another way to cut down the technology costs per microwave system is mass-production for high market-demand applications.

The established microwave applications with high market-demand, are the mobile communications below 3 GHz, the low-noise block (LNB) for private satellite reception in rural areas in Ku-band [3] and advanced-driver assistance systems (ADAS) radar in 77 GHz band [4]. However, the industry plans new mass-market applications in the microwave wavelength regime. Examples can be found in the area of the smart factory initiative [5, 6]. Here, the intent of massive distribution of sensors and wireless connectivity in manufacturing plants. With the tremendous amount of sensor data and connectivity to vast computation power, manufacturing processes can make their own decisions forming so-called artificial intelligence. As a result, future factories achieve a higher automation level, making them more sustainable and competitive. The NaLoSysPro project [7] uses the 250 MHz wide, and unlicensed Industrial-Medical-Scientific (ISM) band at 24 GHz for a localization radar sensor. NaLoSysPro is described in this work and is part of the smart factory initiative.

Another field of emerging mass-market microwave applications are wireless communication systems. Wireless data traffic will grow at an average annual growth rate of 46 % between 2017 and 2022, reaching 77.5 EB per month by this year [8]. The expected growth of wireless data traffic has motivated the International Telecommunications Union (ITU) to investigate applications in frequency bands above 6 GHz [9]. The fifth generation of wireless communications (5G) foresees peak data-rates of 20 Gb/s. Therefore, a feature of the 5G new radio access technology is the employment of mm-wave frequency bands ranging up to 52.6 GHz [10]. However, the infrastructure costs for new wireless communication systems are enormous. For example, the cumulative capex costs for the 5G network infrastructure in Great Britian for 80 % coverage is forecasted to be higher than 40 billion£ [11]. As well as the capex costs the system performance is crucial to attract a large amount

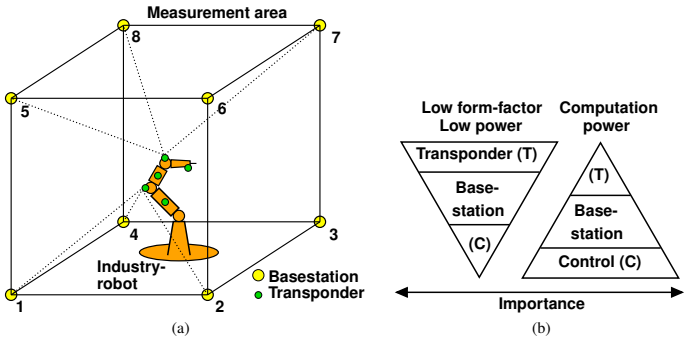

Fig. 1: Cooperative localization system setup. (a) Arrangement of a localization measurement area with example object. (b) Difference in form-factor, power consumption, and computation power of the key-elements in a localization system.

of service subscribers to justify the high effort. That is why the trend to even higher data-rates makes larger bandwidths inevitable for future wireless communications. The project DataRace investigates a front-end covering the W-band from 75-to-110 GHz for a demonstrated 100 Gb/s wireless link.

1.1.1 Project NaLoSysPro

Cooperative localization based on FMCW radar [12, 13] is becoming more popular in the industrial environment, such as smart factories. These include control units that know at all-times, where the robot and the product are located in three dimensions utilizing an accuracy of sub-decimeter. This information is used for various functions such as collision detection or screwdriver angle control. The aim is to lower the scrap reject for more cost-effective, sustainable and competitive manufacturing processes. However, higher local positioning technology distribution for even smaller tools and applications can only be achieved through low cost, low power consumption, and small form factor. High accuracy and immunity due to multipath propagation in complex environments, require large modulation bandwidths, which can be found in the microwave frequency range. The 24 GHz ISM band with 250 MHz modulation bandwidth, is well-suited for sufficient accuracy.

The project entitled NaLoSysPro (german, NahfeldLokalisierung von Systemen in Produktionslinien) aims at a cooperative localization system in manufacturing processes. Cooperative localization systems are based on the secondary radar principle. It uses basestations with known absolute positions, forming the boundaries of the localization area, as shown in Fig. 1a. A localization system consists of the three devices transponder, basestation, and a central control unit (Fig. 1b). The transponders must have the lowest form factor and the lowest power consumption to enable flexible distribution to an object. For example, a cubic measurement area is equipped in each corner with a base station. The objects (i.e., an industry robot) to be located are within this measuring range. Radar transponders are attached to each object so that at least three base stations have a line of sight

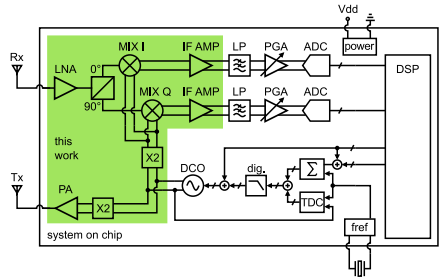

Fig. 2: Highly integrated radar transceiver realized as a CMOS system-on-chip solution with very small amount of external components for low-cost applications.

connection with the transponder. For the base stations and the central control unit, the form factor is less or even unimportant, respectively. In contrast, the computing power in the central control unit must be highest. At the beginning of an absolute distance measurement between one base station and one transponder, clock synchronization between each two has to be done as described in [14]. Low data-rate transmission between base station and transponder for the local oscillator (LO) synchronization is done by frequency-modulated signals in the 24 GHz ISM band. Therefore, the transponder is truly wirelessly operated, apart from the power supply, which makes the system a so-called self-organizing localization network. After successful synchronization, the distance measurement by the FMCW principle is executed. Finally, with cross-bearing, the absolute position in three dimensions of the transponder can be calculated by a central calculation unit, which is connected to all base stations.

In order to enable the mass-production of the transponder, it must serve a wide range of application scenarios. Furthermore, the front-end should have high gain to serve for distances larger than 30 m. The maximum allowed equivalent radiated isotropic power (EIRP) in the 24 GHz ISM band is 20 dBm.

Nanometer complementary metal-oxide-semiconductor (CMOS) technologies are now an attractive choice for microwave applications, due to its sufficient performance and highest possible integration density among the different semiconductor technologies [15]. Therefore, highly integrated CMOS system-on-chip solutions are uniquely cost-effective in mass-production, due to the small number of external components. Furthermore, CMOS operates at considerably lower current consumption than classical microwave semiconductor technologies like Silicon-Germanium or Indium-Phosphide [16]. In addition to the modulation bandwidth, the phase noise and the linearity of the modulation ramp are crucial for high accuracy. An empirical expression for phase noise provides the Leeson's equation [17] and reads

$$L(f_m) = 10\log\left[\frac{2kT}{P_{sig}}\left(\frac{f_c}{2Q_L f_m}\right)^2\right]. \tag{4}$$

Higher Q-factors Q_L of the resonator tanks lead to a lower phase noise in oscillator circuits, but only finite Q-factors are possible. Therefore, the minimum phase noise is bounded. For superior phase noise performance, phased-locked loops (PLL) are used to stabilize analog voltage-controlled

oscillators (VCO). In [18] it has been shown that varactors in nanometer CMOS are very sensitive to analog control voltages. Thus, voltage fluctuations increase the phase noise of analog VCOs. All-digital phased-locked loops (ADPPL) avoid analog tuning voltages and external low-frequency filters compared to analog counterparts. The digital-controlled oscillator (DCO) is tuned by a digital word and acts as a digital to frequency converter. Overall, the ADPLL approach allows for higher integration along with high immunity to noise and thanks to the digital interface for frequency modulation and flexible digital linearization. A fundamental mm-wave ADPLL with linearization is demonstrated in 65 nm CMOS at 60 GHz with -90 dBc phase noise [19]. However, a divide-by-32 chain is needed here consuming 28 mW in total, while the output driver power amplifier (PA) consumes 41 mW. In [20] is shown that the generation of microwave signals at lower frequencies combined with frequency multipliers results in better phase noise compared to a signal generation at fundamental frequencies. However, a frequency multiplication desires for many power and area consuming multipliers as well as an output driver. In [21] quadrature voltage-controlled oscillators are used for subharmonic mixing of 24 GHz by a 12 GHz LO signal to low intermediate frequency (IF). It is proposed that this method produces less LO radio-frequency (RF) feedthrough and, due to this, lower self-mixing effect. [22–24] extends the prior subharmonic approach to a IQ receiver with a multi-phase (8) VCO. Apart from the relatively large area consumption for the multi-phase VCO, the VCO cores must all be uniformly loaded by a frequency divider. This sums up to 34 mW of power consumption for the dividers, although only one is used for operation in a PLL.

The intended highly integrated radar transponder, as depicted in Fig. 2, uses a 12 GHz fundamental ADPLL for signal generation. The frequency doubler in the receiver part offers truly balanced operation with output power larger than 5 dBm for downconversion, resulting in a low self-mixing effect. In the transmit part, a frequency doubler co-optimized with an output stage for output power larger than 13 dBm, and overall power-added-efficiency of more than 20 % is integrated. This allows for the best trade-off regarding phase noise, power consumption, and area consumption for the LO signal generation in the 24 GHz ISM-band. Furthermore, the receiver consists of an in-phase and quadrature-phase (IQ) path enabling the phase measurement in the radar system. As a result, only the antennas, the reference oscillator, and the DC power supply must be provided externally to complete the radar transponder, which enables a small form factor as well as low costs. To further facilitate integration, all circuits should operate from the same 1.2 V supply voltage. In this work, the 24 GHz front-end circuits for the NaLoSysPro project are discussed, which are marked green in Fig. 2.

1.1.2 Project DataRace

Modern wireless communication systems aim at high data-rates towards 100 Gb/s, to serve the ever increasing trend of high data traffic. The global mobile data traffic will exceed in year 2023 the 100 EB (Exabyte, Exa=10^{18}) [25].

The design of such systems follows two different approaches. Either one uses a single channel (SISO: Single-Input Single-Output) with high bandwidth and operating frequency or combine multiple parallel channels width moderate bandwidth and operating frequency (MIMO: Multiple-Input Multiple-Output). A 2x2 MIMO system is implemented in 90 nm CMOS, which achieves 108 Mb/s at a operating frequency of 5 GHz [26]. The authors address besides their implementation, one issue of MIMO systems, namely crosstalk mechanisms. Uniquely if the MIMO system is fully integrated on one chip, the crosstalk can be tremendous. In [27], the authors present a 60 GHz polarization MIMO system, which uses two orthogonal polarizations in the same frequency channel. The over-

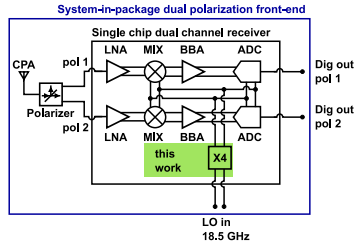

Fig. 3: DataRace single chip system in package 100 Gb/s wireless communication system.

the-air measurements show up to 24 Gb/s with 16 quadrature-amplitude modulation (QAM) and 10 cm air transmission. A SISO approach using 28 GHz and 32 antenna elements is demonstrated by [28, 29].

The project DataRace (Fully Integrated Dual-Polarized Antenna Array with Ultra-Wideband Single-Chip CMOS Receiver) investigtes a receiver front-end covering the W-band from 75 to 110 GHz. The envisaged bandwidth of 35 GHz results in a relative bandwidth of

$$bw_{rel} = \frac{BW}{f_c} = \frac{35GHz}{92.5GHz} \approx 38\%. \tag{5}$$

Fig. 3 shows the system-in-package (SiP). The SiP approach enables scalable two-dimensional receiver arrays, which can improve link-budged, whenever it is needed. It comprises of a circular-polarized antenna (CPA), a polarizer, and a single-chip dual-channel receiver (SCDCR). The polrizer seperates two orthogonal polarizations and feeds two individual receivers. As a result, DataRace employs two channels with 35 GHz of bandwidth, to achieve 100 Gb/s of total wireless datarate. The SCDCR integrates two channels comprising of low-noise amplifier, down-conversion mixer, baseband broadband amplifier, and analog-to-digital converter (ADC) on a single chip. In order to relax the integration and scaling of the SiP, the LO signal is fed at a frequency of 18.5 GHz. The expected losses of the LO distribution network are significantly lower at a quarter of the needed frequency of 74 GHz. That is why, the SCDCR has a frequency quadrupler to multiply the incoming LO signal of 18.5 GHz to 74 GHz. The resulting 74 GHz LO-signal downconverts the front-end bandwidth to 1-36 GHz IF, which is beneficial, due to the presence of 1/f-noise below 1 GHz. A baseband broadband amplifier amplifies the IF signal, such that the ADCs noise figure is not perishing the reception. The ADC is clocked as well by the 74 GHz signal, which further eases scaling and integration because no additional clocking signal has to be distributed within the receiver array.

Amplifiers are key building blocks for a communication system. Fig. 4a shows a simplified equivalent circuit for a transistor in common source configuration. The input behaves like a series R-C low-pass circuit, while the output behaves like a parallel R-C low-pass circuit. In broadband circuit design, the bandwidth is mainly limited by the low-pass behaviour of the transistors, which will not allow for bandwidths in the microwave range. For microwave frequencies, the parasitic R-C elements of the transistors are large and wavelengths are in the range of the electrical distances between the circuits, causing impedance mismatching and reflections, lowering the signal being present at the load. For maximum power transfer between the sources and loads, impedance transformations for conjugated matching are necessary. Fig. 4b depicts the concept for conjugated matching of a

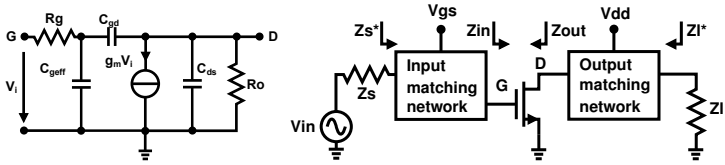

Fig. 4: nMOS microwave amplifier. (a) Simplified equivalent circuit of a nMOS in common source configuration. (b) Amplifier circuit with conjugate input and output matching to maximize power transfer.

microwave amplifier. A matching network transforms Z_{in} to Z_s^* and Z_{out} to Z_l^*. Z_s and Z_l are not necessarily a real impedance such as 50 Ohm and can be as well an imaginary impedance as in matching between amplifier stages. The simplest approach of a matching network is the L-network comprising two lumped elements being a reactance and a susceptance [2]. Both the reactance and susceptance can be either negative or positive, thus forming a second-order low- or high-pass filter. However, additional requirements on the matching networks narrow down the flexibility for design. For example one requirement is, that the decoupling of a DC supply realized by a bias-tee diplexer, which can be a reused L-network. Another requirement is a high-pass behavior since it can damp the higher intrinsic transistor gain at lower frequencies, which improves the stability of a microwave amplifier. The L-netowrk between the source impedance and load impedance forms a higher-order band-pass. The amplifier is tuned to a pass-band frequency, where the signal power is transferred from the source to the load. With the described L-network the matching is valid for a narrow bandwidth, which is typically around 10 % [30]. Thus, for this project higher order matching networks such as a cascade of L-networks or transformers to realize the bandwidth of 38 % are investigated. Particularly challenging is here, that the transistors must offer enough intrinsic gain to overcome the potential losses of a cascade L-network.

The project DataRace employs a 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology, which has nMOS transistors with ft/fmax of 350/370 GHz [31]. It has sufficient performance in mm-wave frequency bands and has the highest possible integration density among all semiconductor, since it is a CMOS process. That means, the whole RF and IF analog front-end circuit can be integrated on a single chip, which lowers the overall integration costs. Furthermore, the technology offers two ultra-thick copper layers in the back-end of line (BEoL) (ca. 3 µm), which is promising for high-Q passives for matching networks with low losses. Finally, the SiP integrates by a polymer-metal technology the front-end chip with the polarizer and the circular polarized antenna.

1.2 Outline of this work

This work is organized as follows. Chapter 2 discusses the NaLoSysPro and DataRace system design. Based on link-budget calculations the performance requirement for the circuit blocks are provided Chapter 3 focusses on the CMOS technology details for the 65 nm bulk and 22 nm FDSOI process. Chapter 4 covers the 24 GHz front-end circuits developed for the NaLoSysPro project. It comprises

the entire receiver chain, transmitter, and LO doubler. The next chapter covers the LO quadrupler is described in detail and how the circuit is optimized in the context of the DataRace project. The concluding remarks are given in Chapter 6.